DON BOSCO INSTITUTE OF TECHNOLOGY, BANGALORE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(NBA Accredited Department)

ACADEMIC YEAR 2021-2022 (ODD SEM)

Question Bank

SUBJECT	:	**VLSI DESIGN**
SUB CODE	:	**18EC72**
SEM	:	**VII**

Module 1

1. Explain the operation of NMOS transistor with its cross sectional view? CO-1 RBT-L1
2. Explain the operation of CMOS Logic? CO-1, RBT-L1
3. Write a note on the operation of assertive high switch & assertive low switch? CO-1, L1
4. Explain any 2 non ideal VI characteristics of MOS Transistors? CO1, L2
5. Write a note on pass transistors & it's working? CO1, L2

Module 2

6. Design 3 i/p NOR Gate using cmos logic? CO2, L2
7. Write a note on β ratio effects of mos transistor CO1; L2
8. Write a note on DC transfer characteristics of cmos transistor? CO1, L2
9. Write a note on β ratio effects of mos transistor? CO1, L2
10. Explain the operation of D latches & D flipflops? CO3, L2

Module 3

11. Explain the n-well CMOS fabrication process CO1, L1
12. Reduce the Scaling factor for Drain current, Power dissipation, Gate oxide and Power density in a constant field scaling model CO1, L2
13. Write a note on two different types of Scaling models CO1, L2
14. Explain MOSFET Oxide capacitance with schematic representation CO1, L3

Module 4

15. Write short note on Voltage generator CO3, L1

16. Write short note on voltage sense amplifier CO3, L2

17. Derive the expression for (Charge up event)rise time and (Charge down event)fall time for pass transistor CO3, L3

18. Write a note on linear delay model and Elmore delay model CO3, L3

19. Find the output capacitance for 3 input nand gate with W/L ratio of PMOS 2:1 and NMOS 3:1 CO3, L3

Module 5

20. Explain all the Manufacturing test principles CO5, L1

21. Explain the working principle of BIST CO5, L2

22. Explain Scan based design CO5, L2

23. With the help of diagram, explain the conceptual Random access memory organization CO4, L2

24. Explain Logic verification principles CO5, L1

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Department of Electronics and Communication Engineering

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SEMESTER: VII
Sub: VLSI Design -18EC72
Assignment-1, Academic Year- 2021-22

	Group 1	
01	Explain the operation of NMOS transistor with its cross sectional view?	L2, C01
02	Explain the operation of CMOS Logic?	L2, C01
03	Write a note on the operation of assertive high switch & assertive low switch?	L2 C01
04	Write a note on tri state inverter & explain its operation ?	L1 C01
05	Explain the concept of 2:1 mux design using cmos logic & 2:1 inverting mux tri state inverter?	L2 C01
06	Explain any 2 non ideal VI characteristics of MOS Transistors?	L1 C01
	Group 2	
01	Explain the operation of PMOS transistor with its cross sectional view?	L2 C01
02	Design 3 i/p NAND Gate using cmos logic?	L2 C01
03	Write a note on transmission gates & its working?	L1 C01
04	Write a note on tri state buffer & explain its operation ?	L2 C01
05	Explain the concept of 4:1 mux design using tri state inverter?	L2 C01
06	Explain ideal VI characteristics of MOS transistor?reduce expression of Ids?	L2 C01
	Group 3	
01	Design 3 i/p NOR Gate using cmos logic?	L2, C01
02	Design the combinational logic circuit for y=(AB+CD)'	L2 C01
03	Write a note on pass transistors & its working ?	L2 C01

HSD

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04	Write a note on β ratio effects of mos transistor?	L2 C01
05	Explain the operation of latches & flipflops?	L2 C01
06	Write a note on DC transfer characteristics of cmos transistor?	L1 C01

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SEMESTER: VII
Sub: VLSI Design -18EC72
Assignment-2, Academic Year- 2021-22

Q. No.	QUESTIONS	Bloom's level
	Group 1	
1	Explain the n-well CMOS fabrication process	L2
2	Explain Short-channel effects.	L2
3	Explain MOSFET Junction Capacitance with schematic representation	L2
4	Explain Logic verification principles	L1
5	Write a note Isolation fabrication technique.	L1
	Group 2	
1	Explain the p-well CMOS fabrication process	L2
2	Write a note on two different types of Scaling models	L3
3	Explain MOSFET oxide capacitances with schematic representation	L2
4	Write a note on BIST & BILBO	L2
5	Explain the Photolithography and Czochralski methods.	L2
	Group 3	
1	Explain Layout design rules.	L2
2	Explain the Techniques involved in CMOS fabrication design process	L2
3	Explain the Twin tub & Triple well CMOS fabrication process	L2
4	Explain Manufacturing test principles	L1
5	Write a note on scan based design	L1

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SEMESTER: VII **Sub: VLSI Design** **Sub Code:18EC72**

Assignment -3

Q. No.	QUESTIONS	Bloom's level
	Group 1	
1	With the help of diagram Explain The conceptual Random access memory organization	L2
2	List out the various configuration of Static RAM cell	L2
3	Explain the working of write operation of SRAM cell with timing diagram	L2
4	Explain the working of read operation of SRAM cell with timing diagram	L2
5	List out the various configuration of DRAM cell	L1
	Group 2	
1	Write short note on Voltage generator	L2
2	Write short note on voltage sense amplifier	L3
3	Explain the different circuit design for convention CMOS latches	L3
4	Explain the circuit design for convention CMOS Flip-flops	L2
5	Explain resettable Flip-flops with diagrams	L2
	Group 3	
1	Explain resettable latches with diagrams	L2
2	Derive the expression for (Charge up event)rise time and (Charge down event)fall time for pass transistor	L2
3	Write three stage depletion load NMOS dynamic shift register circuit driven with two phase clocking	L2
4	Write a note on linear delay model and Elmore delay model	L2
5	Find the output capacitance for 3 input anand gate with W/L ratio of PMOS 2:1 and NMOS 3:1	L3

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ACADEMIC YEAR 2021-2022(ODD SEM)

SURPRISE TEST–I

SUBJECT	:	VLSI Design
SUB CODE	:	18EC72
SEM	:	VII

	ANSWER ANY TWO EACH QUESTION CARRIES 5M	
01	Explain MOS theory	L2,C01
02	Represent the expression y=(A+B+C).D	L2,C01

ASb

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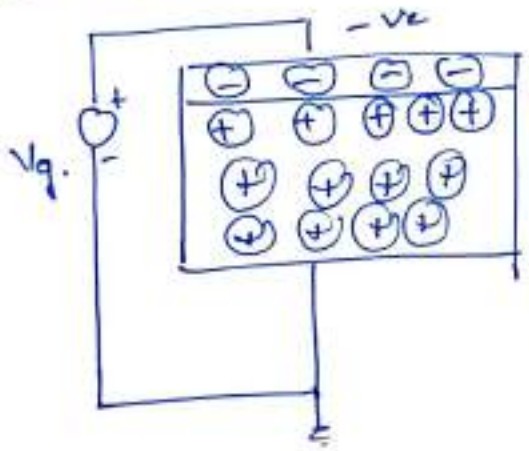
Surprise test -1 [VLSI Design - 18EC72]

- 5M -

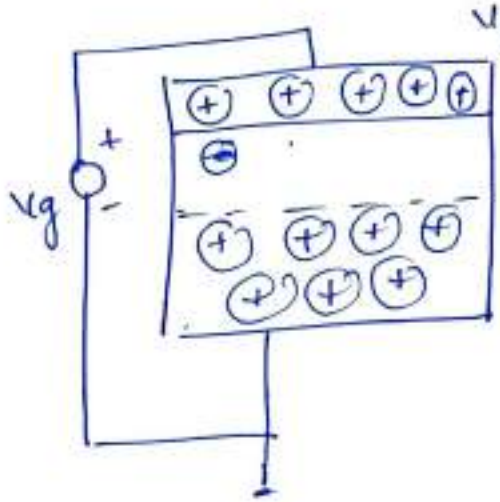
(1) Explain NMOS theory.



$V_{gs} < 0$

(a) Accumulation.

- 2M -



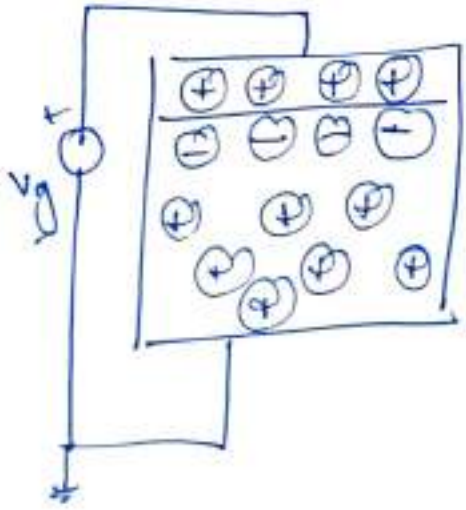
Vg is positive

$V_g < V_{th}$

Depletion region

(b)

- 2M -



$V_g > V_{th}$

Inversion region - 2M -

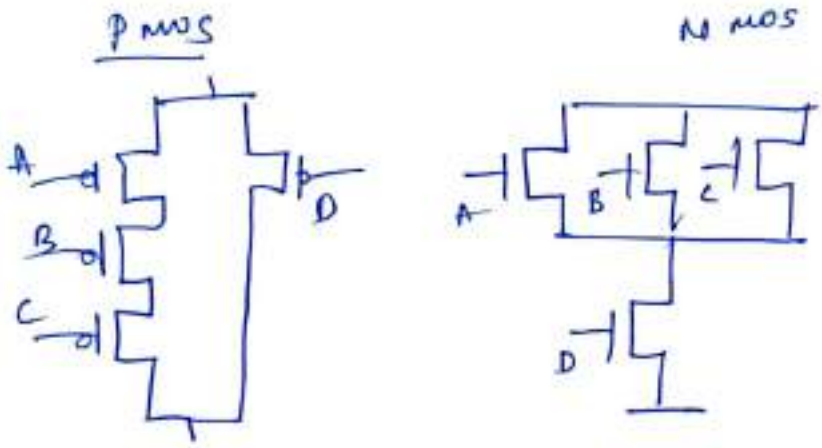
(c)

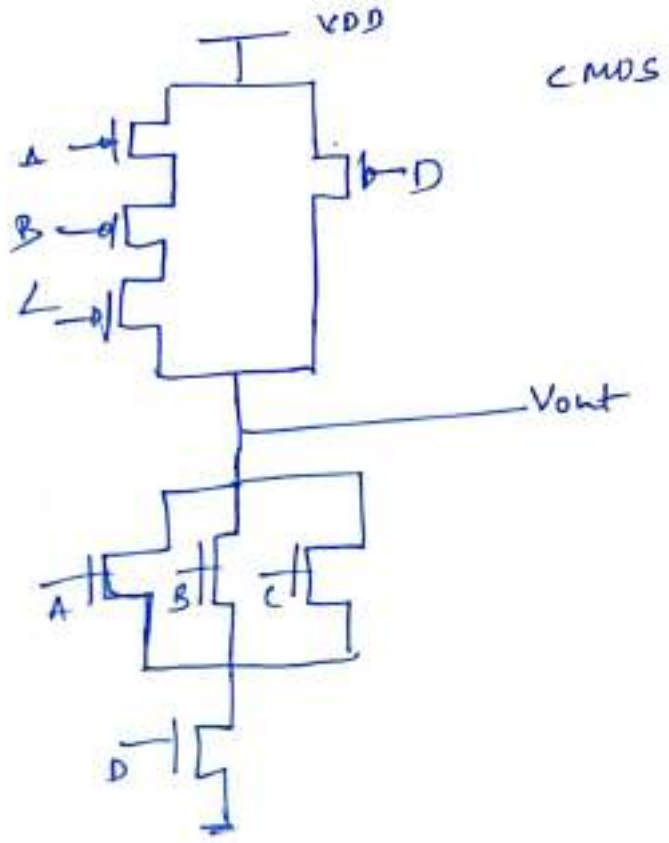
Explanation

- 2M -

$\overline{Y} = \overline{(A+B+C)D}$

-5 M-





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ACADEMIC YEAR 2021-2022(ODD SEM)

SURPRISE TEST–II

SUBJECT	:	VLSI Design
SUB CODE	:	18EC72
SEM	:	VII

	ANSWER ANY TWO EACH QUESTION CARRIES 5M	
01	Explain Layout design rules	L2,C02
02	Explain twin tub fabrication process	L2,C01
03	Manufacturing test principles	L1,C05

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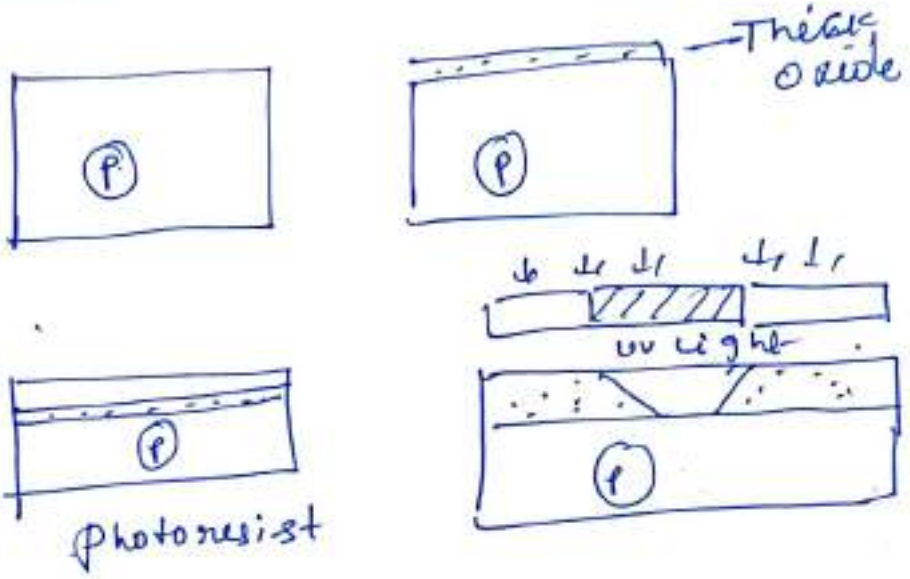
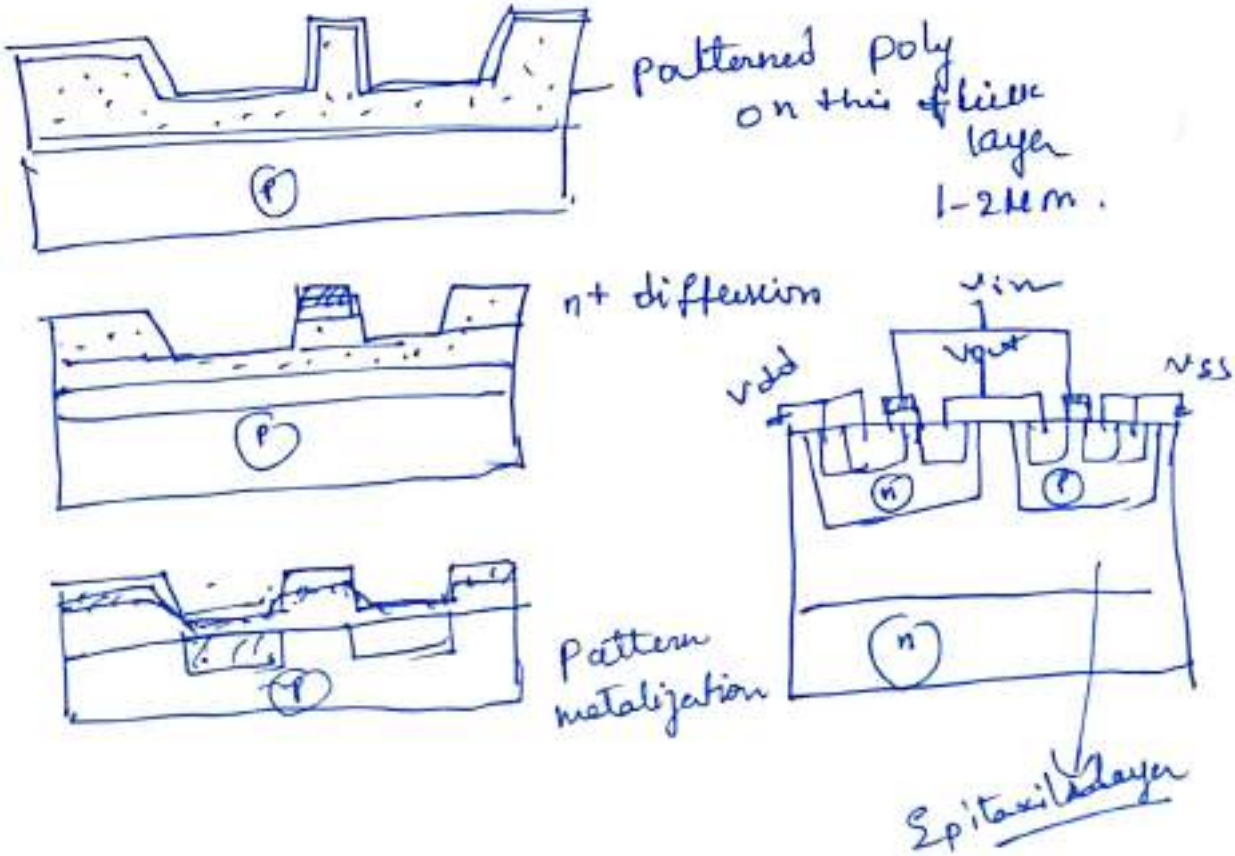
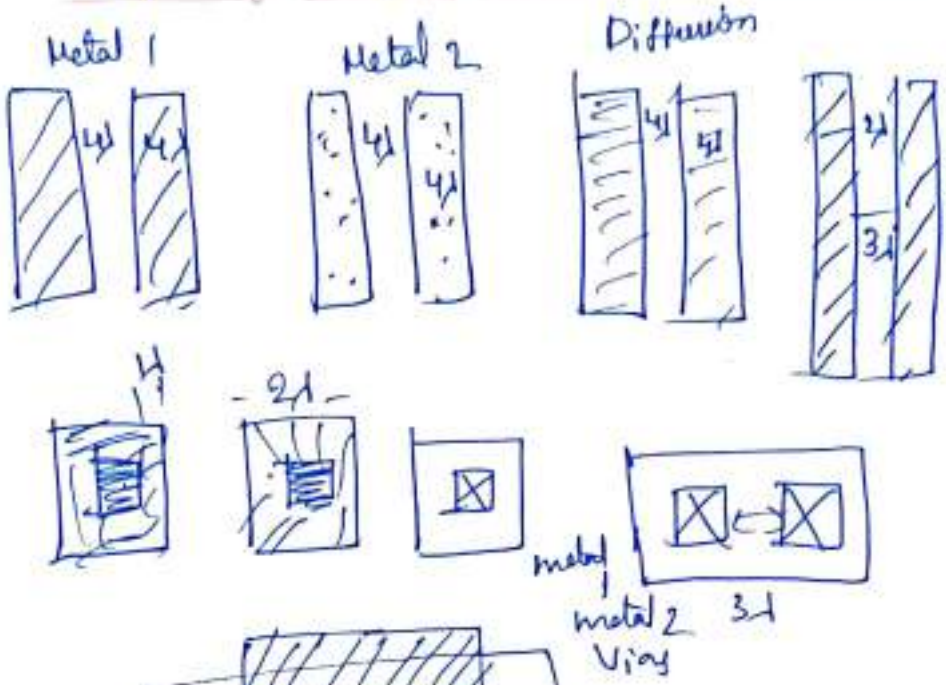
Surprise test -2 VLSI design - 18EC72

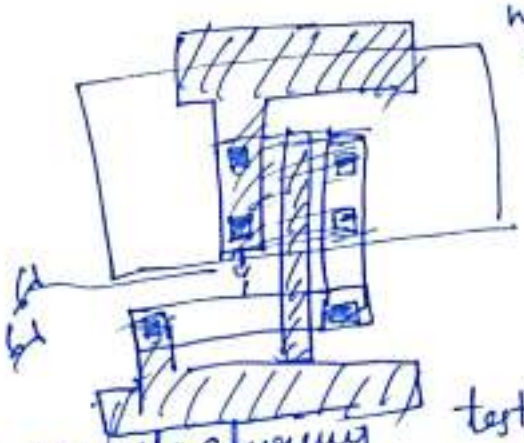
Twin tub fabrication process -5M.





② Layout design rules. —5M—





λ based design rule

③ manufacturing test principles —5M

① fault model
② Struct at fault
Short ckt & Open ckt faults.
Explaination in detail 2½

② Observability
③ Controlability
④ fault coverage
⑤ Automatic test pattern Generation (ATPG)
⑥ Delay fault testing —2½M—

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SEMESTER: VII
Sub: VLSI Design
Quiz-1, Academic Year-2021-22

1. VLSI technology uses _____ to form integrated circuit.
   a) **transistors**
   b) switches
   c) diodes
   d) buffers
2. Medium scale integration has _____
   a) ten logic gates
   b) fifty logic gates
   c) **hundred logic gates**
   d) thousands logic gates
3. _____ architecture is used to design VLSI.
   a) system on a device
   b) single open circuit
   c) **system on a chip**
   d) system on a circuit
4. Physical and electrical specification is given in _____
   a) architectural design
   b) logic design
   c) system design
   d) **functional design**
5. Gate minimization technique is used to simplify the logic.
   a) **true**
   b) false
6. nMOS devices are formed in
   a) p-type substrate of high doping level
   b) n-type substrate of low doping level
   c) **p-type substrate of moderate doping level**
   d) n-type substrate of high doping level
7. In depletion mode, source and drain are connected by _____
   a) insulating channel
   b) **conducting channel**

c) Vdd
d) Vss

8. What is the condition for non saturated region?
a) Vds = Vgs – Vt
b) Vgs lesser than Vt
c) **Vds lesser than Vgs – Vt**
d) Vds greater than Vgs – Vt

9. As source drain voltage increases, channel depth _____
a) increases
b) **decreases**
c) logarithmically increases
d) exponentially increases

10. CMOS inverter has _____ output impedance.
a) **low**
b) high
c) very high
d) none of the mentioned

VLSI Design - quiz 1 18ec72

55	9.6	Active
Responses	Average Score	Status

1. USN (0 point)

55
Responses

Latest Responses
"1DB18EC140"
"1DB18EC164"
"1DB18EC146"

Update

1 respondents (2%) answered **1DB19EC403** for this question.

2. NAME (0 point)

55
Responses

Latest Responses
"Sonika D"
"HARSHITHA GK"
"suprith n c"

Update

8 respondents (15%) answered M for this question.

3. SECTION (0 point)

55
Responses

Latest Responses
"C"
"C"
"C"

4. VLSI technology uses _____ to form integrated circuit. (1 point)

98% of respondents (54 of 55) answered this question correctly.

a) transistors	54 ✓
b) switches	1
c) diodes	0
d) buffers	0

5. Medium scale integration has _____ (1 point)

100% of respondents (55 of 55) answered this question correctly.

a) ten logic gates	0	
b) fifty logic gates	0	
c) hundred logic gates	55	✓
d) thousands logic gates	0	

6. _____ architecture is used to design VLSI (1 point)

96% of respondents (53 of 55) answered this question correctly.

a) system on a device	1	
b) single open circuit	1	
c) system on a chip	53	✓
d) system on a circuit	0	

7. Physical and electrical specification is given in _____ (1 point)

96% of respondents (53 of 55) answered this question correctly.

a) architectural design	0	
b) logic design	1	
c) system design	1	
d) functional design	53	✓

8. Gate minimization technique is used to simplify the logic (1 point)

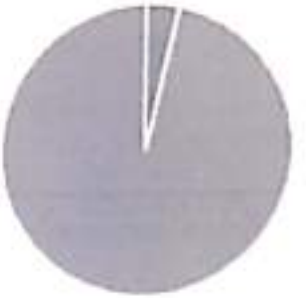
100% of respondents (55 of 55) answered this question correctly.

a) true	55	✓
b) false	0	

9. nMOS devices are formed in _____ (1 point)

96% of respondents (53 of 55) answered this question correctly.

) p-type substrate of high dopin...	2	
b) n-type substrate of low dopin...	0	
c) p-type substrate of moderate...	53	✓
d) n-type substrate of high dopi...	0	



10. In depletion mode, source and drain are connected by _____ (1 point)

100% of respondents (55 of 55) answered this question correctly.

insulating channel	0	
b) conducting channel	55	✓
c) Vdd	0	
d) Vss	0	

11. What is the condition for non saturated region? (1 point)

80% of respondents (44 of 55) answered this question correctly.

Vds = Vgs – Vt	11	
b) Vgs lesser than Vt	0	
c) Vds lesser than Vgs – Vt	44	✓
d) Vds greater than Vgs – Vt	0	

12. As source drain voltage increases, channel depth _____ (1 point)

96% of respondents (53 of 55) answered this question correctly.

a) increases	0	
b) decreases	53	✓
c) logarithmically increases	0	
d) exponentially increases	2	

13. CMOS inverter has _____ output impedance. (1 point)

100% of respondents (55 of 55) answered this question correctly.

a) low	55	✓
b) high	0	
c) very high	0	
d) none of the mentioned	0	

USN | 1 | D | B | | | | | | | |

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Department of ELECTRONICS and COMMUNICATION Engineering

Internal Assessment Test-I Odd Sem AY 2021-22

Course Name: VLSI Design | Course Code: 18EC72 | Date:18/11/2021

Semester & Section: 7[III] (A/B/C) | Max marks: 30 | Time: 3 PM to 4 PM

Note: Answer any Two full questions, choosing only One full question from each Module.
Each full question carry maximum of 15 marks

Q NO	Module-1 Questions	MARKS	CO	RBT
1	a) Write a note on DC transfer characteristics of CMOS transistor.	10M	1	L1
	b.) Write a note on β ratio effects of CMOS transistor.	5M	1	L1
	OR			
2	a) Explain the operation of D latches & D flip flops.	10M	1	L2
	b) Explain steps involved in VLSI Design flow.	5M	1	L2
	Module-2 Questions			
3	a)Design 3 i/p NOR Gate and Nand gate using cmos logic.	8M	1	L3
	b) Design the combinational logic circuit for $y = \overline{AB + CD}$.	7M	1	L3
	OR			
4	a) Write a note on transmission gates .	5M	1	L1
	b) Explain ideal VI characteristics of MOS transistor? Deduce expression of I_{ds}.	10M	1	L2

Name & Signature of Course Instructor

ROOPA K R – Roopa 16/11

Scrutinized by (Name & Signature)

1) Dr. JPP 16/11/2021

2) Dr. CVS 16/11/21

3) HOD- 16/11/2021

Kumbalagodu, Mysore road, Bangalore -74

Department Of Electronics and Communication Engineering

Internal Assessment November 2021

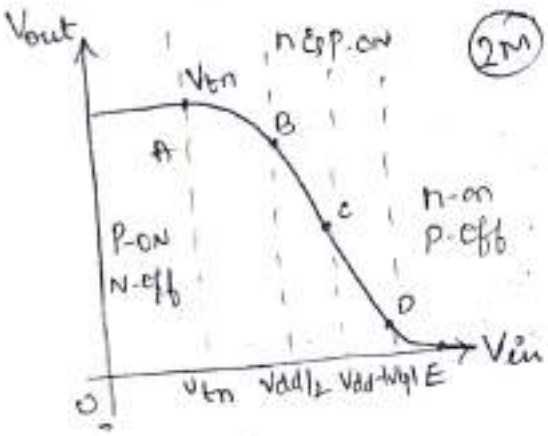
SCHEME OF EVALUATION

Subject: VLSI DESIGN
Sub Code: 18ECT72
Faculty Name: ROOPA.K.R

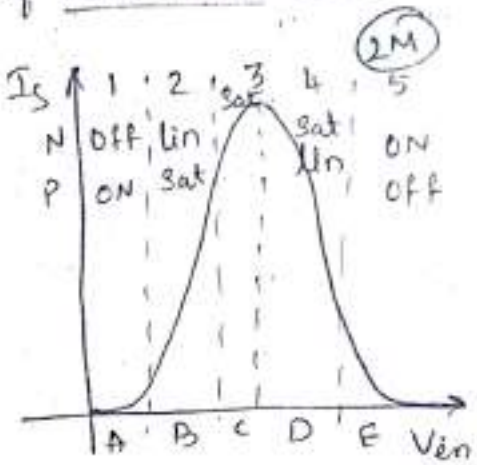
Semester VII th
Max Marks: 30

Q. No	SCHEME & SOLUTION	Marks

1a) Dc transfer characteristics of CMOS transistors :- 10M



(2M)



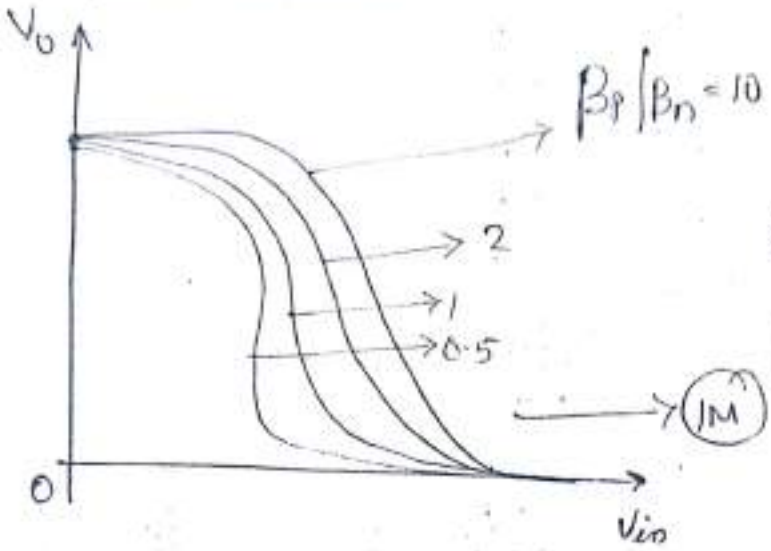
(2M)

(3M)

region	Condition	PMOS	nmos	o/p
A	$0 \le V_{in} \le V_{tn}$	linear	cut off	$V_o = V_{dd}/2$
B	$V_{in} \ge V_{tn}$ & $V_{in} < \frac{V_{dd}}{2}$	Sat	lin	$V_o < V_{dd}/2$
C	$V_{in} = V_{dd}/2$	Sat	Sat	$V_{out} \downarrow$
D	$V_{dd}/2 < V_{in} \le \frac{V_{dd}}{2} - \lvert V_{tp}\rvert$	lin	Sat	$V_o > V_{dd}/2$
E	$V_{in} > V_{dd}/2 - \lvert V_{tp}\rvert$	Cut off	lin	$V_o = 0$

Explanation — 3m → i/p & o/p voltage w.r.t 3 different regions needed. Explanation is

1b) **β Ratio Effects of mos transistor:-**



(1M)

Explanation (1M)

↳ Variation of β factor varies o/p parameter

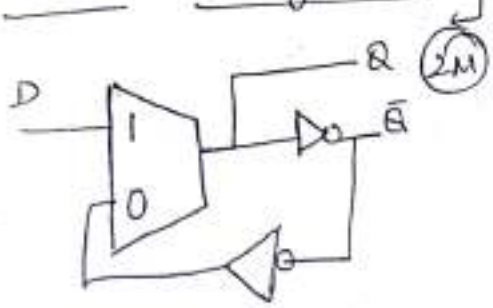
Conditions (3M)

- $\beta_p/\beta_n > 1$ — Hi Skewed inverter
- $\beta_p/\beta_n < 1$ — low Skewed inverter
- $\beta_p/\beta_n = 1$ — normal skew/unskewed.

10M

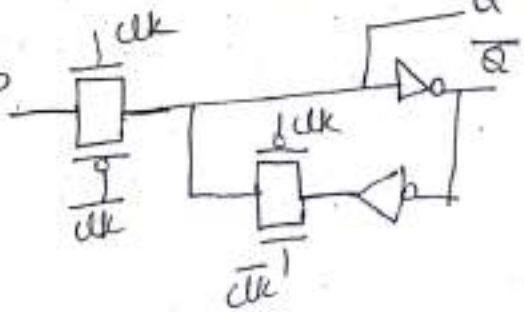
2a) **D latch & DFF**

D latch using MUX :-

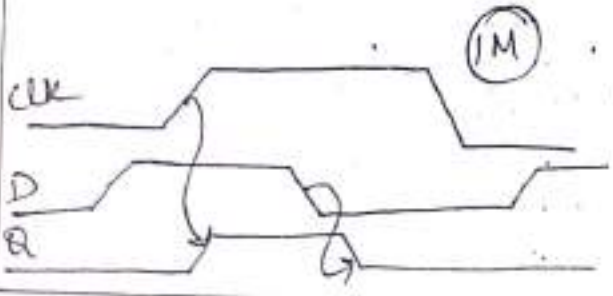


(2M)

D latch using TG :-



(2M)



(1M)

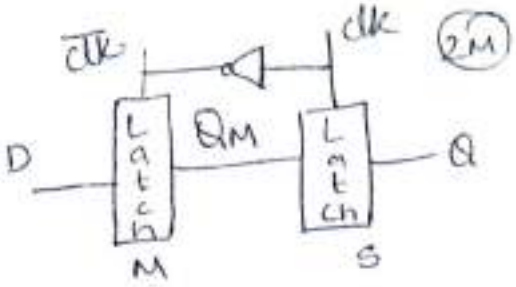
Explanation:

(5M)

when D=0 o/p = 0 wrt clk=1

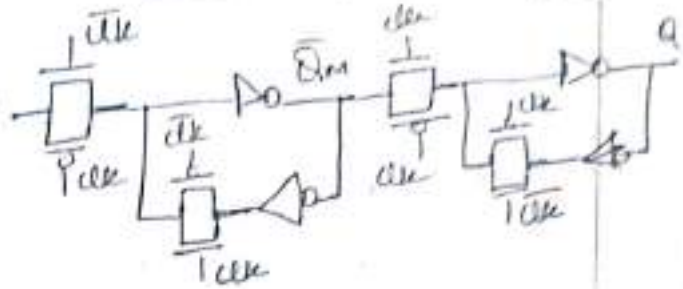
D=1 o/p = 1 clk=1

DFF using latch

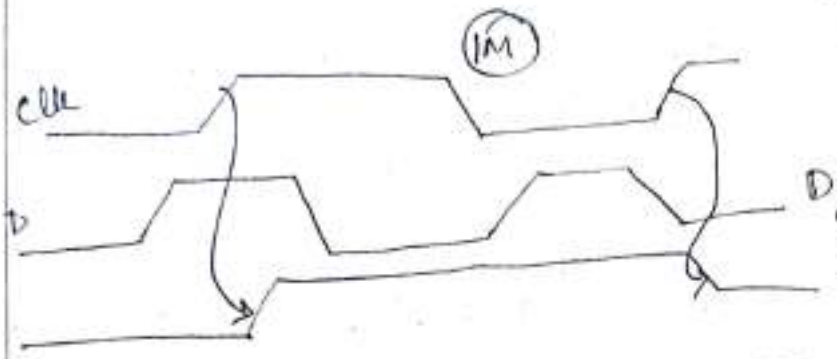


(2M)

DFF using TG:



(2M)



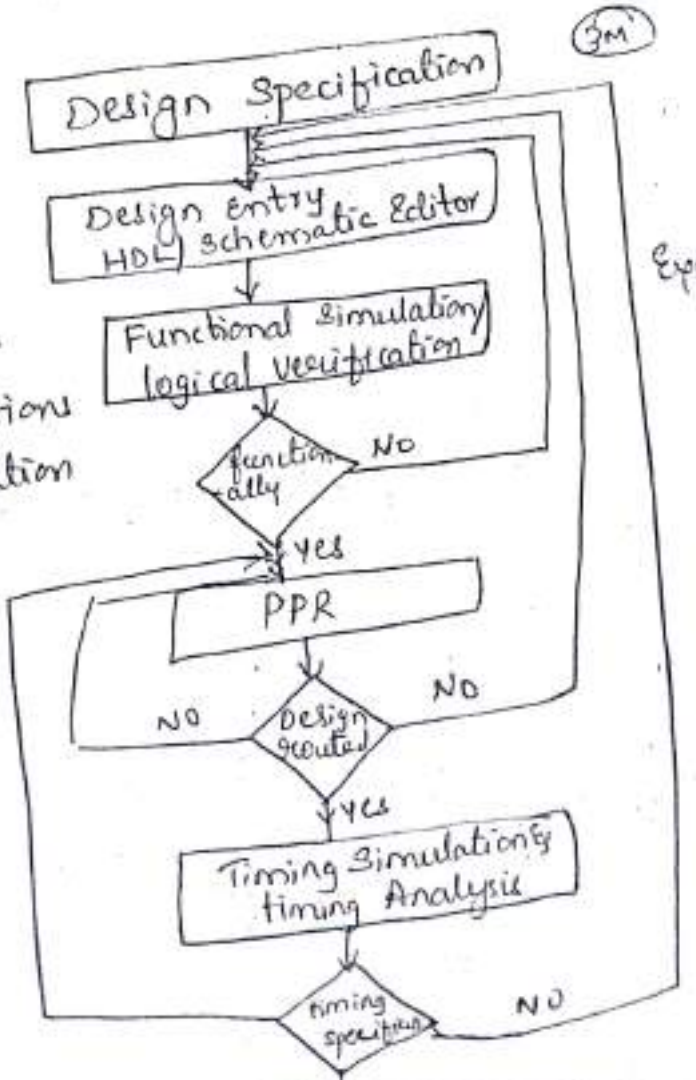
(1M)

Explanation (5M)

D=0 when S=0 M=1 (clk=1) o/p QM=
& when S=1, M=0 (clk=0) o/p

5M

2b)



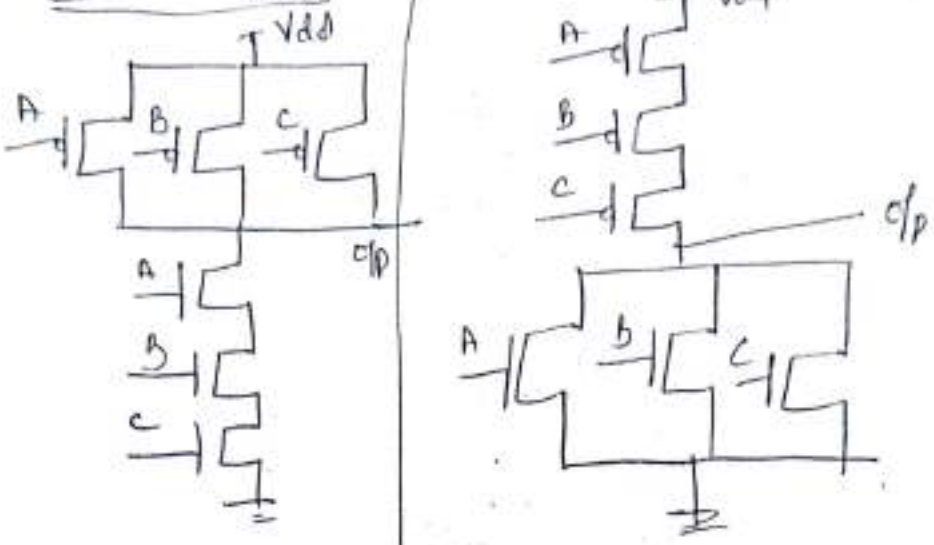
(3M)

Explanation: (2M)

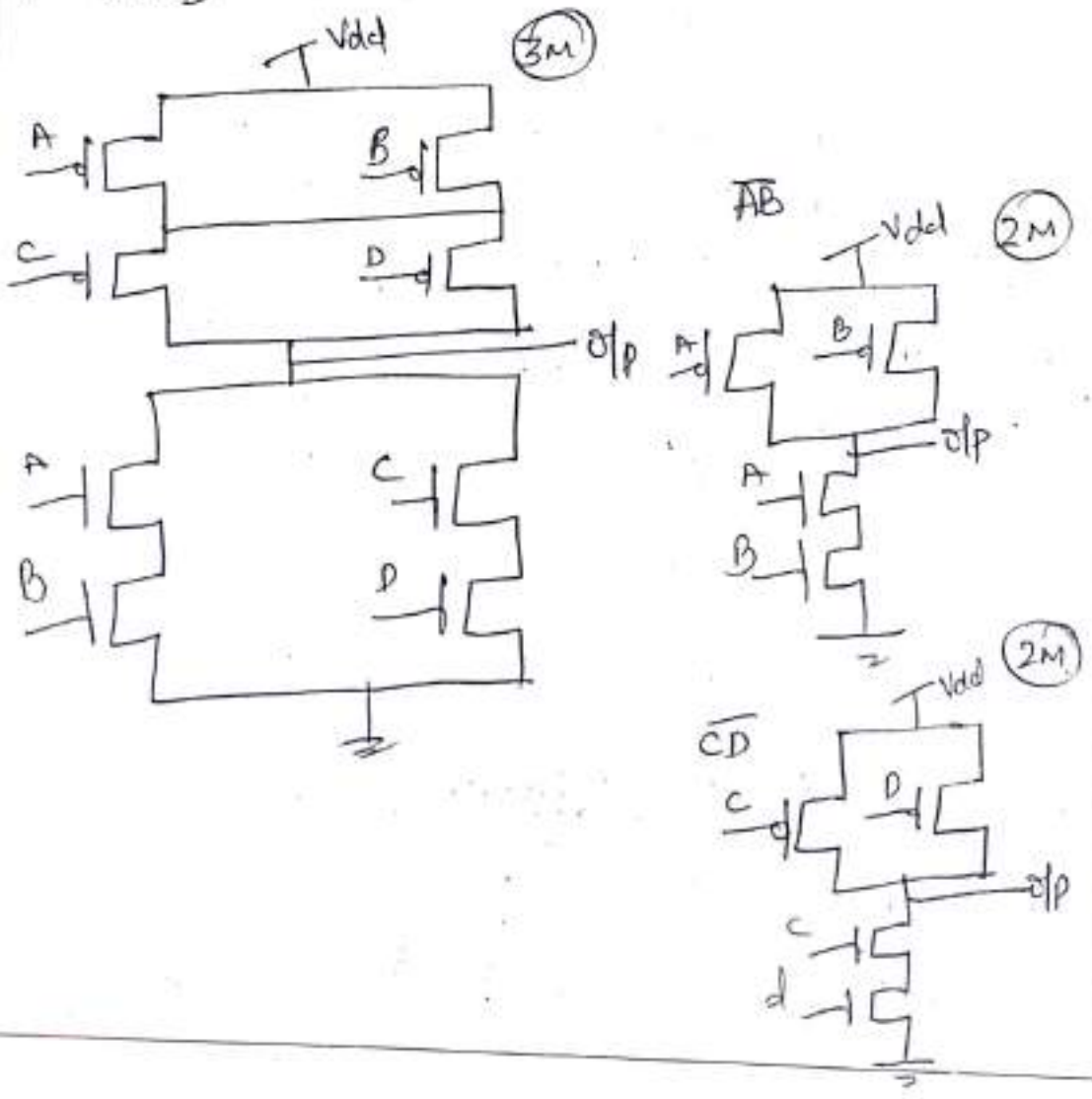
1) I/O specifications
2) area utilization
3) power
4) Routing.

3a) Nand = $\overline{A \cdot B \cdot C}$ & NOR = $\overline{A+B+C}$

(4M) Each

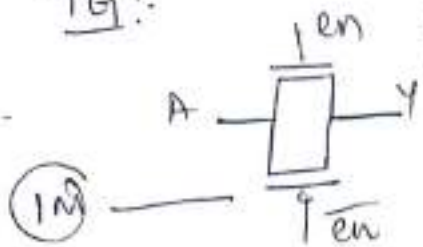


3b) $Y = \overline{AB+CD}$ 7M



5M

4a) TG:



en/$\overline{en}$	A	Y
0/1	0	Z
0/1	1	Z
1/0	0	0
1/0	1	1

Explanation → (2M)

when en=0 o/p = Z irrespective of i/p

en=1 o/p = i/p

10M

4b) VI characteristics of NOS

$Q = C \cdot V$ charge in channel — (1M)

gate capacitance $C_g = \frac{\varepsilon_{ox} \cdot WL}{t_{ox}}$ — (1M)

$V = \mu E$ & $I_{ds} = Q/L/V$ — (1M)

$I_{ds} = \mu C_{ox} \frac{W}{L} \left[V_{gs} - V_t - V_{ds}/2 \right] V_{ds}$ → linear (3M)

$I_{ds} = \beta \left[V_{gs} - V_t - V_{ds}/2 \right] V_{ds}$ [$\because V_{ds} = V_{gs} - V_t$ in sat]

$\beta = \mu C_{ox} \cdot W/L$ & $K = \mu \cdot C_{ox}$ (or) $\beta = \frac{KW}{L}$

$\therefore I_{ds} = \beta/2 \left[V_{gs} - V_t \right]^2$ → saturation. (3M)

$$\therefore I_{ds} = \begin{cases} 0 & \text{cut off} \\ \beta \left[V_{gs} - V_t - V_{ds}/2 \right] V_{ds} & \text{lin} \\ \beta/2 \left(V_{gs} - V_t \right)^2 & \text{sat.} \end{cases}$$

Explanation & diagram (1M)

USN | 1 | D | B | | | | | | |

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Department of Electronics and Communication Engineering

Internal Assessment Test-II

Course Name: VLSI Design | Course Code: 18EC72 | Date:20/12/2021

Semester & Section: VII/A, B& C | Max marks: 30 | Time: 3PM-4PM

Note: Answer any two full questions, choosing only one full question from each Module.
Each full question carry maximum of 15 marks

Q NO	Module-2 Questions	MARKS	CO	RBTL
1	a) Explain step by step n-well CMOS fabrication process	10	CO1	L2
	b) Explain Lambda based layout design rules	5	CO2	L2
	OR			
	a)Reduce the Scaling factor for Drain current, Power dissipation, Gate oxide and Power density in a constant field scaling model	7	CO1	L2
	b)Explain Short-channel& Narrow channel effects with diagrams	8	CO1	L2
	Module-5 Questions			
3	a) Explain all the Manufacturing test principles	10	CO5	L1
	b)Explain the working principle of BIST	5	CO5	L2
	OR			
4	a) Explain Scan based design	7	CO5	L1
	b) Explain MOSFET Oxide capacitance with schematic representation	8	CO1	L2

Mrs. RKR
Mrs. SG
Mrs. BAB
Name & Signature of Course Instructor

Scrutinized by (Name & Signature)

1) Dr. JPP 18/12/2021

2) Dr. CNS 18/12/21

3) HOD- 17.12.21

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DON BOSCO INSTITUTE OF TECHNOLOGY

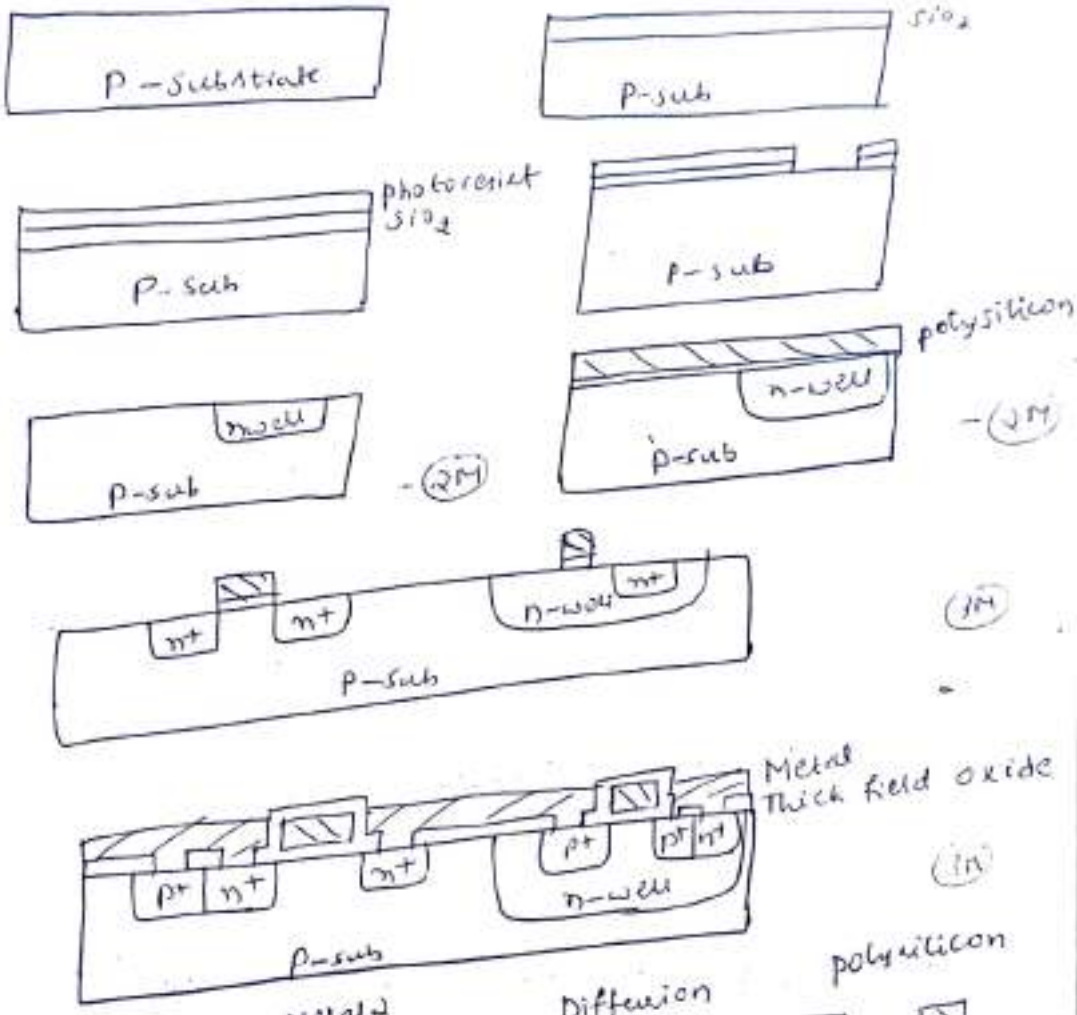
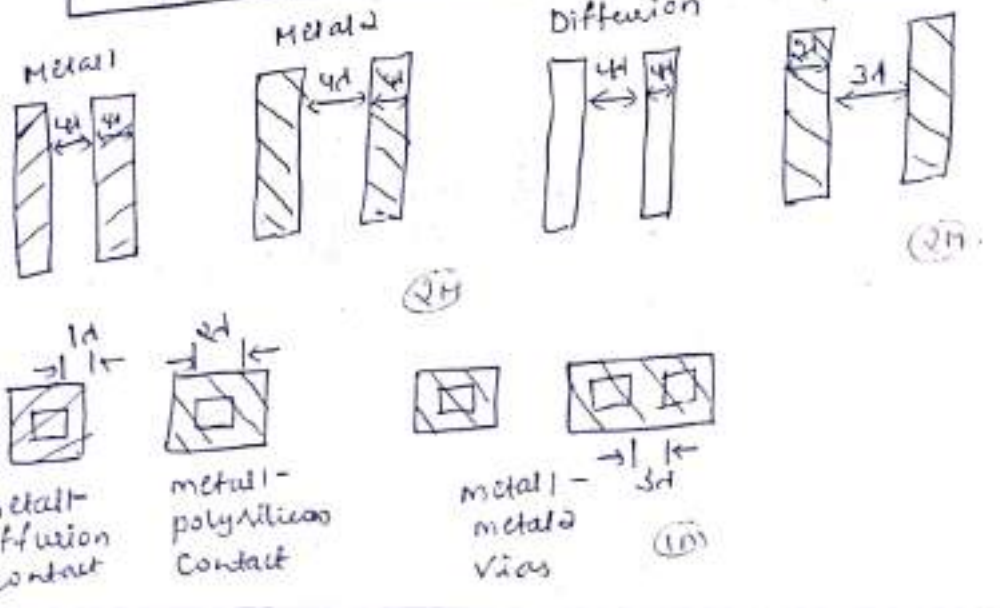
Department Of Electronics and Communication Engineering

Internal Assessment Test – 1 / 2 / 3

SCHEME OF EVALUATION

Name of The Course: VLSI Design | Course Code: 18EC72 | Semester: VII

Max Marks: 30 | Faculty Name: RKR | SG | BAR | Date: 20/12/2021

Q.No	SCHEME & SOLUTION	Marks
1 a)	 – (2M) – (2M) – (10M) – (3M) – (3M)	10M
1 b)	 (2M) (2M) (1M)	5M

Q. No	SCHEME & SOLUTION

2 a) Drain Current :

$$I_{d(sat)}' = \frac{K_n'}{2}\left[2(V_{gs}' - V_T')\cdot V_{DS}' - V_{DS}'^2\right] \quad (3M)$$

$$= \frac{K_n}{2S}\left(2(V_{gs} - V_T)V_{DS} - V_{DS}^2\right] = \frac{I_{D(sat)}}{S}$$

Power Dissipation :

$$P' = I_D' V_{DS}' = \frac{1}{S}\cdot I_D \times \frac{1}{S}\times V_{DS} = \frac{1}{S^2} I_D \cdot V_{DS} \quad (2M)$$

$$P' = P/S^2 \quad (1M)$$

Gate oxide : $C_g = W.L.C_{ox} = \left(W\cdot\frac{1}{S}\right)(L\cdot 1/S)(C_{ox}.S)$ (2M)

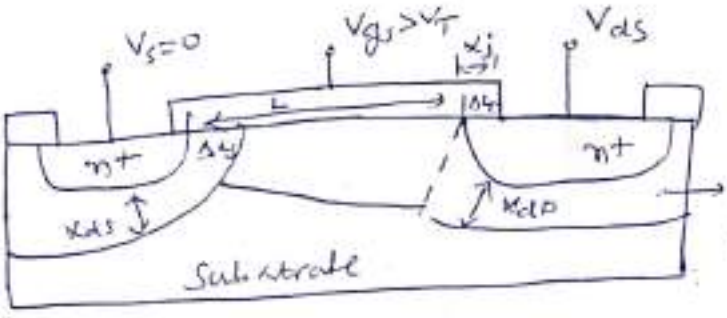
$$C_g = \frac{1}{S}\cdot L\cdot W\cdot C_{ox}$$

Power Density :-

$$P'/Area' = P/Area \quad (1M)$$

2 b) Short-channel effects :

1. Electron Drift characteristics in channel
2. Modification of Threshold voltage.



(2M)

Marks

↳ Due to channel length shortening, effective channel length is reduced.

↳ Carrier velocity in channel is func of normal electric field component. (1M)

↳ Threshold vtg of short channel MOSFET is

$V_{To(short\ channel)} = V_{To} - \Delta V_{To}$

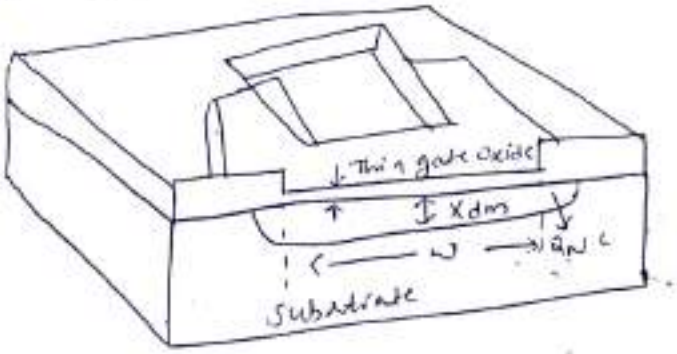
Narrow channel effects:

↳ Actual threshold voltage of a device is larger than that predicted. (1M)

(1M)

$V_{To(Narrow\ channel)} = V_{To} + \Delta V_{To}$

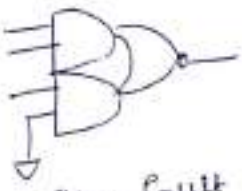
↳ Threshold voltage increases as a result of extra depletion region.



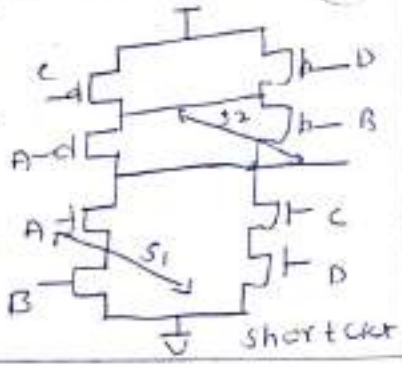
(1M)

3a) i. Fault Models — Stuck-at faults; Short/open ckt model (3M)

SA1 fault



SA0 fault



Q. No	SCHEME & SOLUTION

2. Observability : Ability to determine the signal value at any node by controlling the ckt i/p & observing the o/p

3. Controllability : Ability to establish signal value at any node in a ckt by setting values at circuits i/p's (1M)

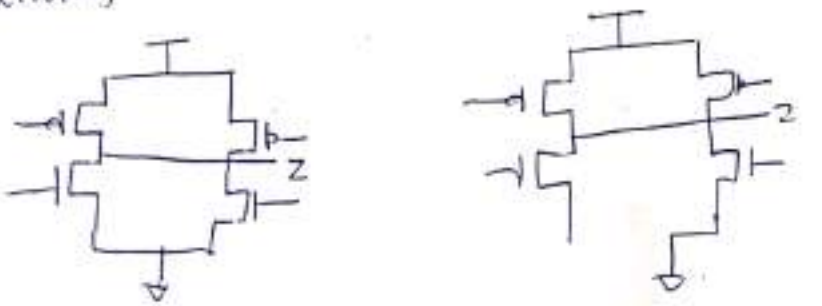
4. Fault coverage :

For Test vectors applied, what % of internal nodes were checked defines the fault coverage. (1M)

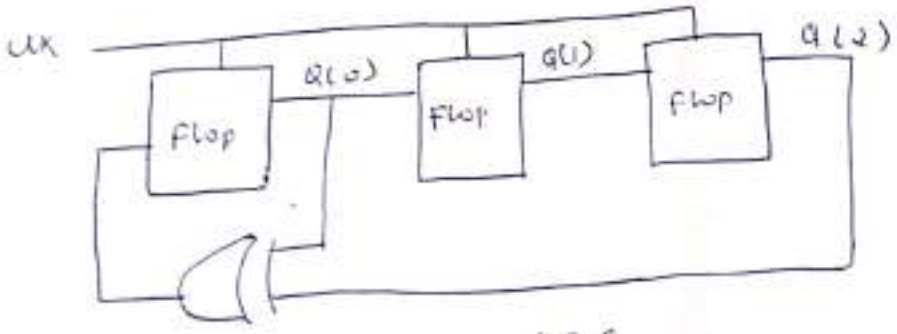
5. ATPG : To reduce the complexity of ckt, ATPG methods are used which achieve excellent fault coverage (1M) (10M)

6. Delay fault Testing :

Failures occur in cmos affects the timing not the functionality. (2M)



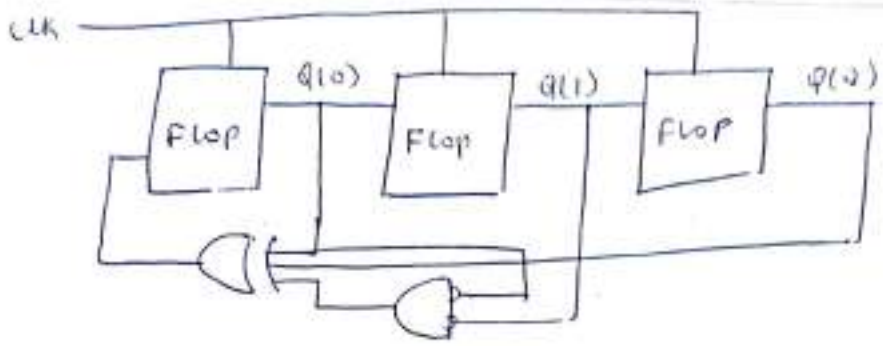
3b)



(2M)

LFSR

Marks



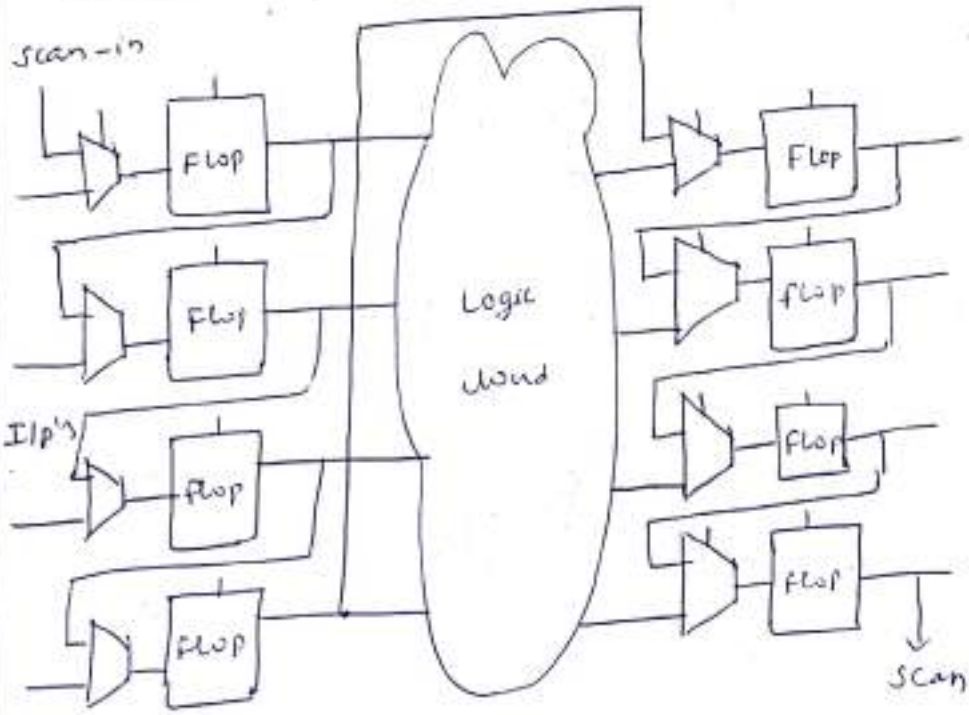
(2M)

(5M)

PRSG

n bit LFSR can be converted into n-bit CFSR by adding n-1 i/p NOR gate (1M)

4a) Serial scan & parallel scan



(3M)

(4M)

(2M)

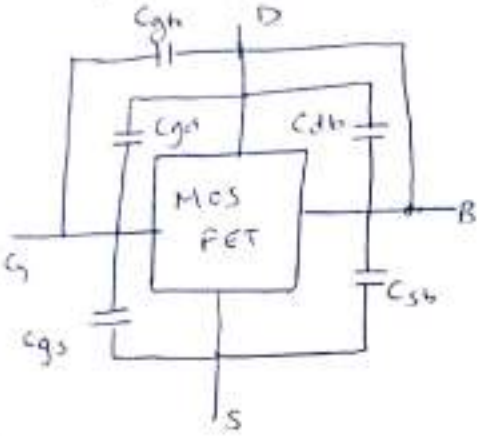
Parallel scan - basic structure

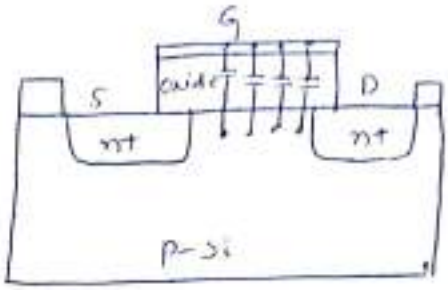
- Scan register is a D FF preceded by mux
- SCAN = 1. Data is loaded from SI pin (2M)
  SCAN = 0, Register stores the data on D input.

Q. No	SCHEME & SOLUTION	Marks

4 b) $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

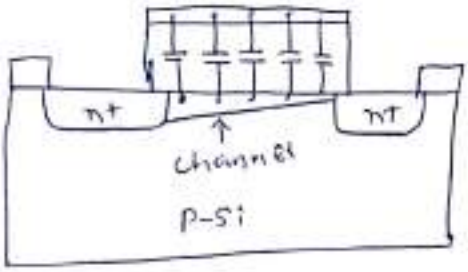
$C_{GS} = C_{ox} \cdot W \cdot L_D$ $\quad C_{GD} = C_{ox} \cdot W \cdot L_D$ (1M)



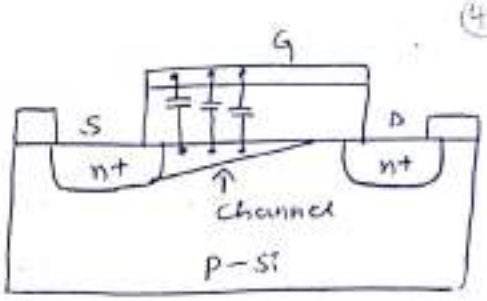


(a) cut off

(4M)



(b) Linear



(c) saturation

(5M)

capacitance	cut off	linear	saturation
C_{gb} (total)	$C_{ox} \cdot W \cdot L$	0	0
C_{gs} (total)	$C_{ox} \cdot W \cdot L_D$	$\frac{1}{2} C_{ox} \cdot WL + C_{ox} \cdot W \cdot L_D$	$C_{ox} \cdot W \cdot L_D$
C_{gc} (total)	$C_{ox} \cdot W \cdot L_D$	$\frac{1}{2} C_{ox} \cdot W \cdot L + C_{ox} \cdot W \cdot L_D$	$\frac{2}{3} C_{ox} \cdot WL + C_{ox} \cdot W \cdot L_D$

(3M)

180

USN | 1 | D | B | | | | | | |

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Department of Electronics and Communication Engineering

Internal Assessment Test-III Odd Sem AY 2021-22

20/1/2022

Course Name: VLSI DESIGN | Course Code: 18EC72 | Date: 17/01/2022

Semester & Section: 7 A, B, C | Max marks: 30 | Time: 02.00 PM TO 03.00 PM

Note: Answer any Two full questions, choosing only One full question from each Module. Each full question carry maximum of 15 marks

Q NO		Module-4 Questions	MARKS	CO	RBTL
1	a	With the help of diagram Explain The conceptual Random access memory organization	8M	4	L1
	b	Explain the working of write operation of SRAM cell with timing diagram	7M	4	L1
		OR			
2	a	List out the various configuration of DRAM cell	8M	4	L2
	b	Write short note on Voltage generator	7M	4	L1
		Module-3 Questions			
3	a	Derive the expression for (Charge up event)rise time and (Charge down event)fall time for pass transistor	8M	3	L2
	b	Explain the different circuit design for convention CMOS latches	7M	3	L1
		OR			
4	a	Write a note on linear delay model and Elmore delay model	8M	3	L1
	b	Find the output capacitance for 3 input NAND gate with W/L ratio of PMOS 2:1 and NMOS 3:1	7M	3	L2

17/01/2022

1 Dr. JPP 17/01/2022

2 Dr. CNS 17/1/22

HoD. 17.1.22

DON BOSCO INSTITUTE OF TECHNOLOGY

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Department Of Electronics and Communication Engineering

Internal Assessment November 2021

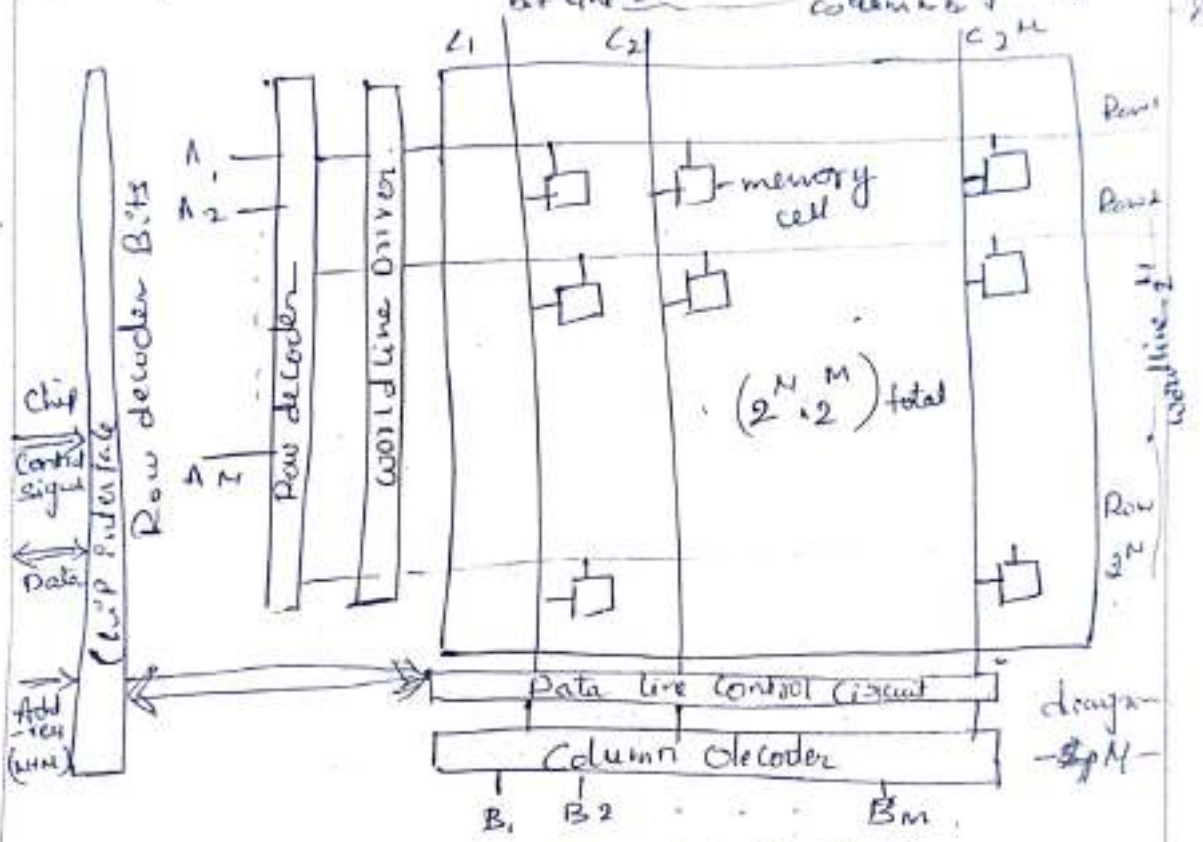
SCHEME OF EVALUATION

Subject: VLSI design
Sub Code: 18EC72
Faculty Name: Bhavya A.B

Semester: VII C
Max Marks: 30

Q. No	SCHEME & SOLUTION	Marks

Conceptual random access memory organization



Conceptual RAM memory array organisation.

(a) total no of memory cell in array: $2^N \times 2^M$.

(b) N → No of rows → 2^N rows totally

(c) M → No. of column → 2^M rows totally

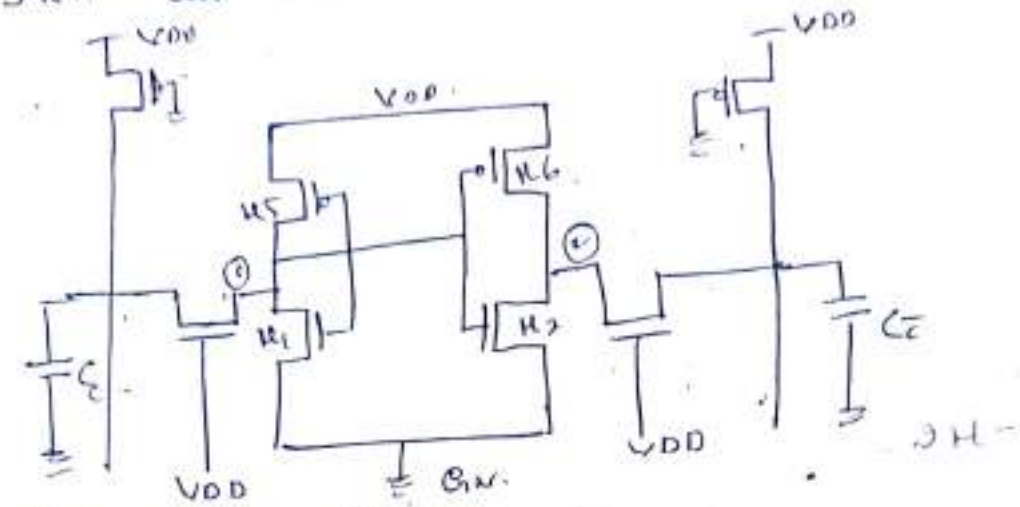
(d) $\overline{CS}$ → control Chip Selects. to control signal.

(e) $\overline{WE}$ → write Enable

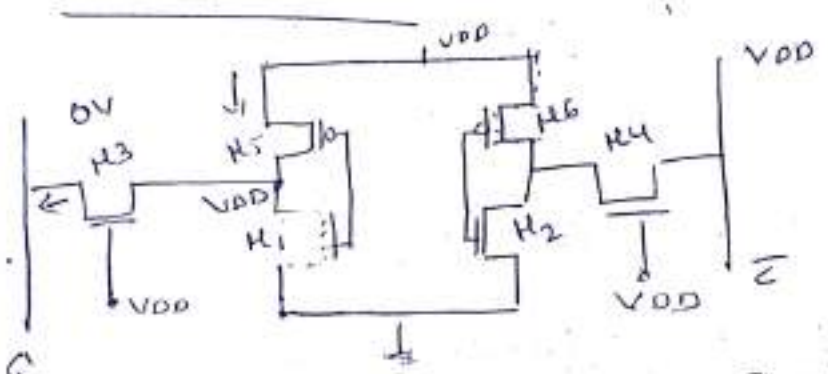
(f) we have address line, data line & control line.

Explanation — 4M —

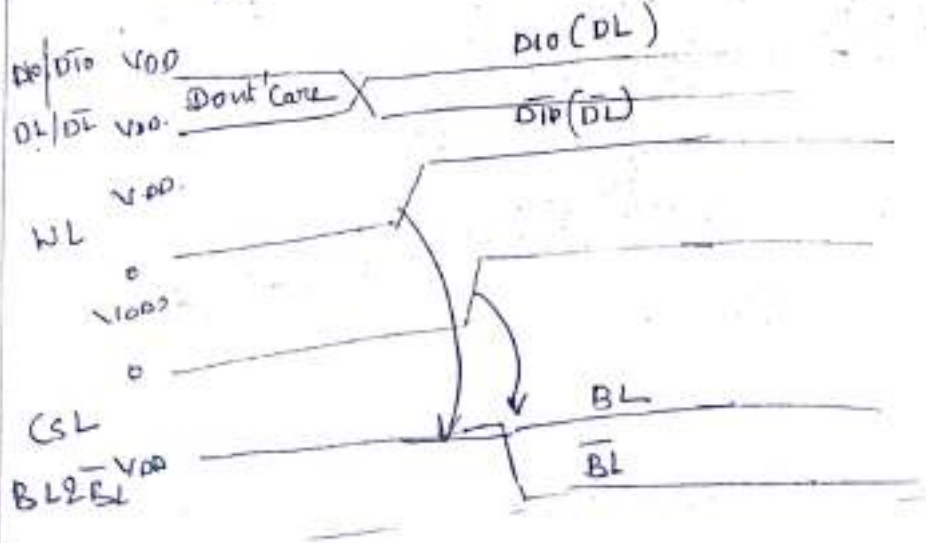
1(b) SRA cell write operation.



Full custom SRM



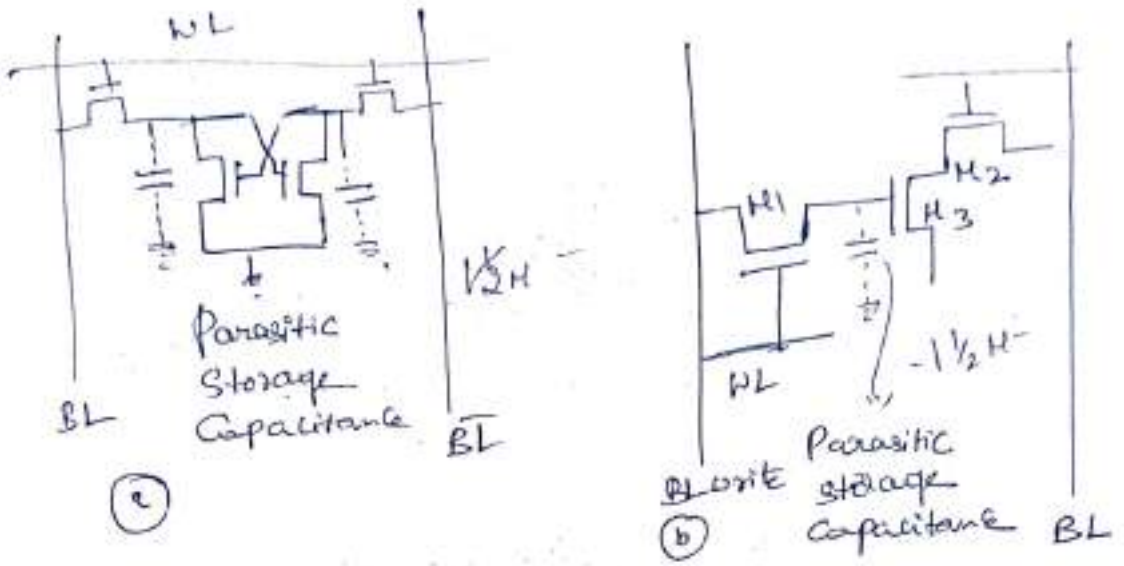
Voltage Level in the SRAM cell at the beginning of write operation



SRAM core operation: write timing

Explanation

(a) DRA Configuration 8M



Various (9) configuration of dynamic cell. Explanation - 2M

(a) (1.) 4 transistor DRAM cell with 2 storage nodes. In write operation WL is Enabled, read operation is enable for read

(c) - 3 three transistor DRAM cell:- only one data for storing,

(b) 2 transistor DRM cell: 1 transistor DRAM cell, 1 is industry std

(d) 1 transistor & 1 capacitor DRAM, for Read & write operation

(5) Voltage generators

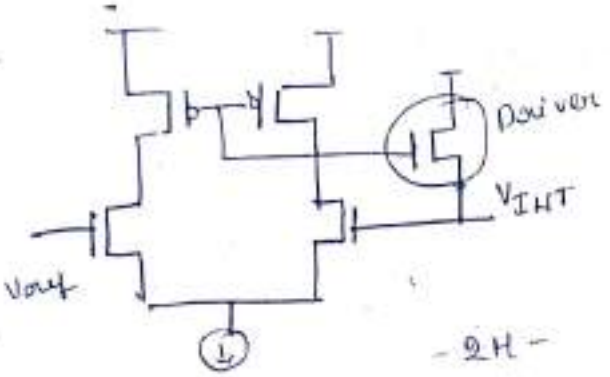
4 types of voltage generators they are.

(a) Internal voltage generator (V_{INT})

(b) Half V_{DD} generator (V_{BL} & V_P)

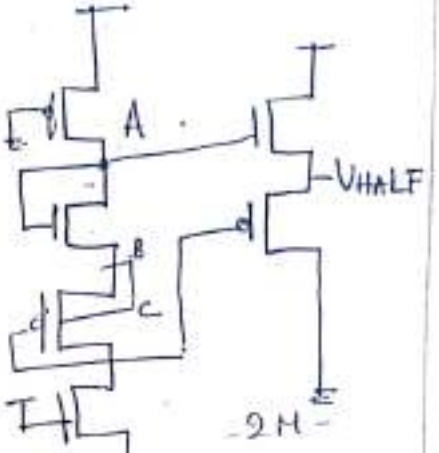
(c) Substrate bias generator (V_{BB})

(d) Boosted voltage generator (V_{PP}) } 1H



2H

Fig a Internal Voltage regulator ckt

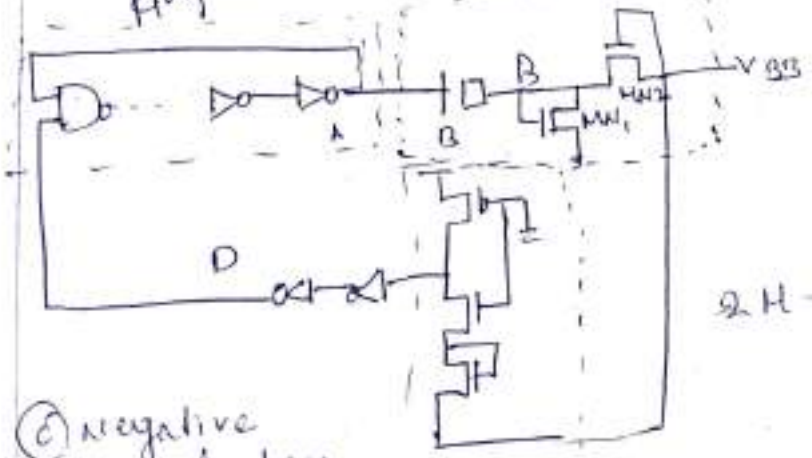


2H

(b) Half V_{DD} voltage generator

Ring oscillator

Charge pump

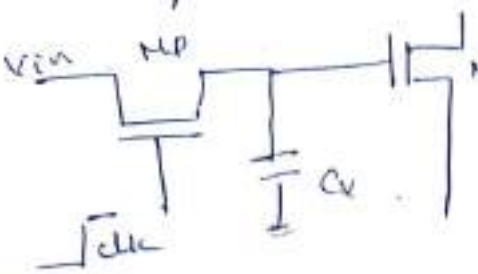


2H

(c) Negative Substrate bias voltage generator - Level detector

SCHEME & SOLUTION	Marks

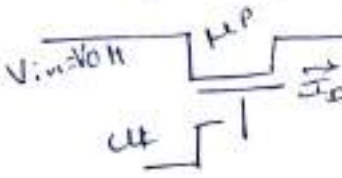
(a) Charge up & charge down event. -3M-



-1/2 M-

(a) Dynamic Logic

Charge up | Logic transfer . $V_{Pn} = V_{OH} = V_{DD}$.



-1/2 M-

MP operates in saturation mode $\Rightarrow V_{gs} > V_{gs} - V_t$ -1M-

$Q_{in} = I_{sat}$.

$C_x \frac{dV}{dt} = \frac{K_n}{2}\left(V_{DD} - V_x - V_{tn}\right)^2$ -1M-

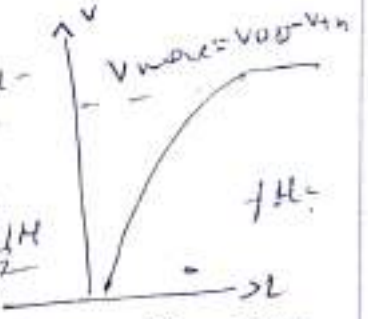
both side

Integrate

$\int_0^t C_x \frac{dV}{dt} = \int_0^{V_x} \left(\frac{K_n}{2}\left(V_{DD} - V_x - V_{tn}\right)^2\right.$ -1/2M-

$\int_0^t dt = \frac{2C_x}{K_n} \int_0^{V_x} \frac{dV_x}{(V_{DD} - V_x - V_{tn})^2}$ -1M-

$t = \frac{2C_x}{K_n}\left[\frac{1}{V_{DD} - V_x - V_{Tn}} - \frac{1}{V_{DD} - V_{tn}}\right]$ -1/2M-



-1M-

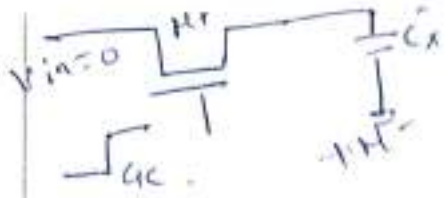
$V_{in} = V_{OH}$, from 0 to V_{DD} pass transistor -1/2M-

gate from 0 to V_{DD}.

$C_x \frac{dV}{dt} = \frac{K_n}{2}\left(2(V_{DD} - V_{tn})V_x - V_x^2\right)$ -1/2M-

$\int_0^t dt = -2\frac{C_x}{K_n} \int_{V_{DD}-V_{tn}}^{V_x} \frac{dV_x}{2(V_{DD} - V_{tn})V_x - V_x^2}$ -1/2M-

$t = \frac{C_x}{K_n(V_{DD} - V_{Tn})}\left[\ln\left[\frac{2(V_{DD} - V_{Tn}) - V_x}{V_x}\right]\right]_{V_{DD}-V_{tn}}^{V_x}$ -1/2M-



$$t = \frac{C_x}{K_n(V_{DD} - V_{Tn})} \ln\left[\frac{2(V_{DD} - V_{in}) - V_x}{V_x}\right]$$

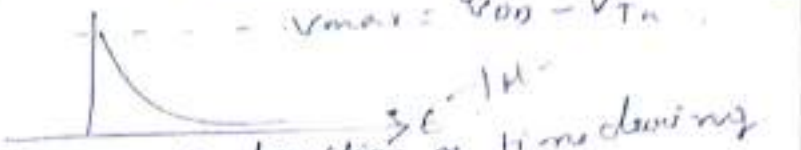


fig: variation of v_x as a function of time during logic 0 transfer

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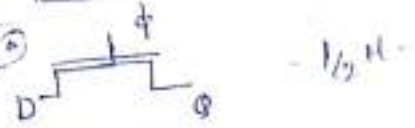
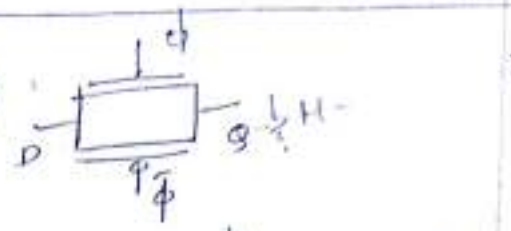
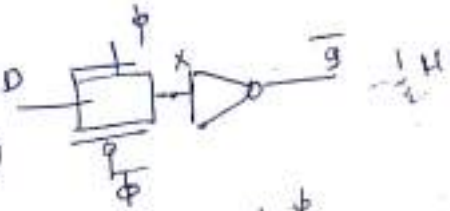
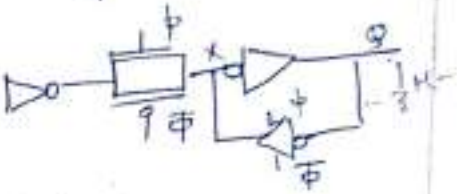
(b) CMOS Latches

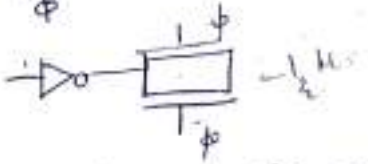
(a) 

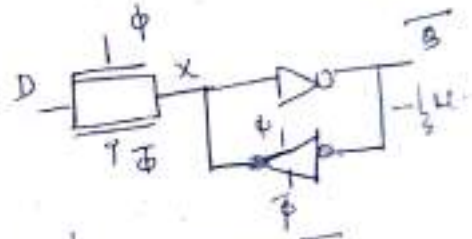
(b) 

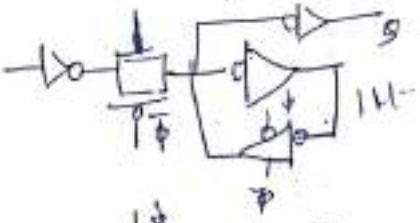
7H

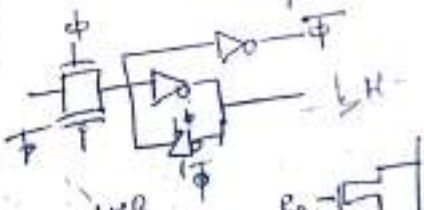
(c) 

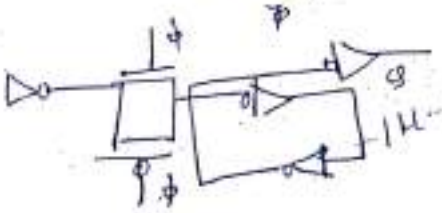
(f) 

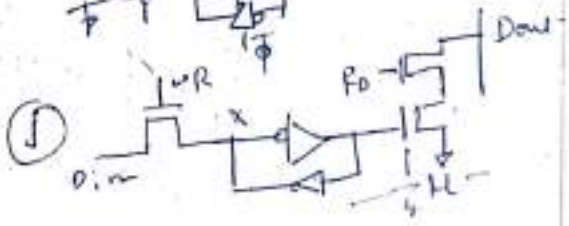
(d) 

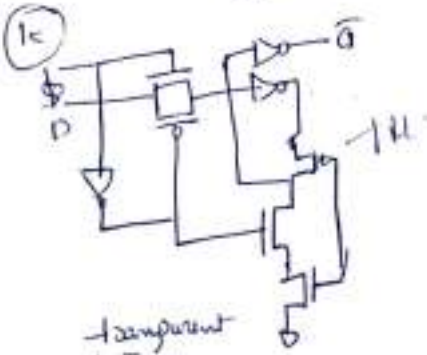
(e) 

(g) 

(h) 

(i) 

(j) 

(k) 

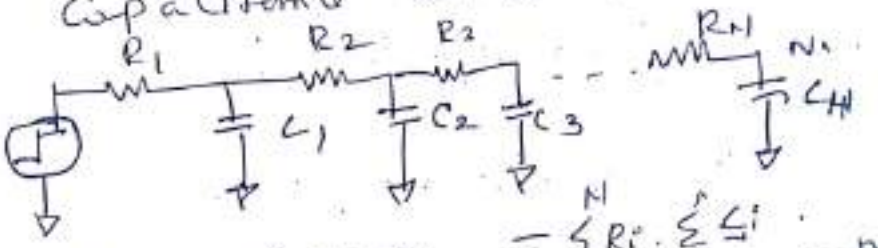
transparent latches

4(a) Linear delay model · Elmore delay model. — 8M

Elmore delay model

(*) Treating on transistor as resistors we consider that chain of transistors can be replaced as an RC Model (ladder).

Elmore delay model estimates the delay of an RC ladder as the sum over each node in the resistance R_{n-1} blw node & supply multiplied by Capacitance on the node. — 2M



$$t_{dP} = \sum_{i} R_i C_i = \sum_{i=1}^{N} R_i \cdot \sum_{j=1}^{i} C_i$$ — 2M

Linear model → logical effort, parasitic delay.

Propogation delay of gate can be written as $d = f + P$ — 1M

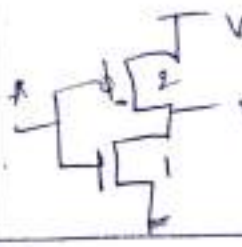
d → effort delay, f → effort delay, P → parasitic delay.

$f = gh$ → electrical effort — 1M

f → effort delay

$$h = \frac{C_{out}}{C_{in}}$$

$$g = \frac{\text{slope of delay of gate}}{\text{slope of delay of Inverter}}$$ — 1M



— 1M

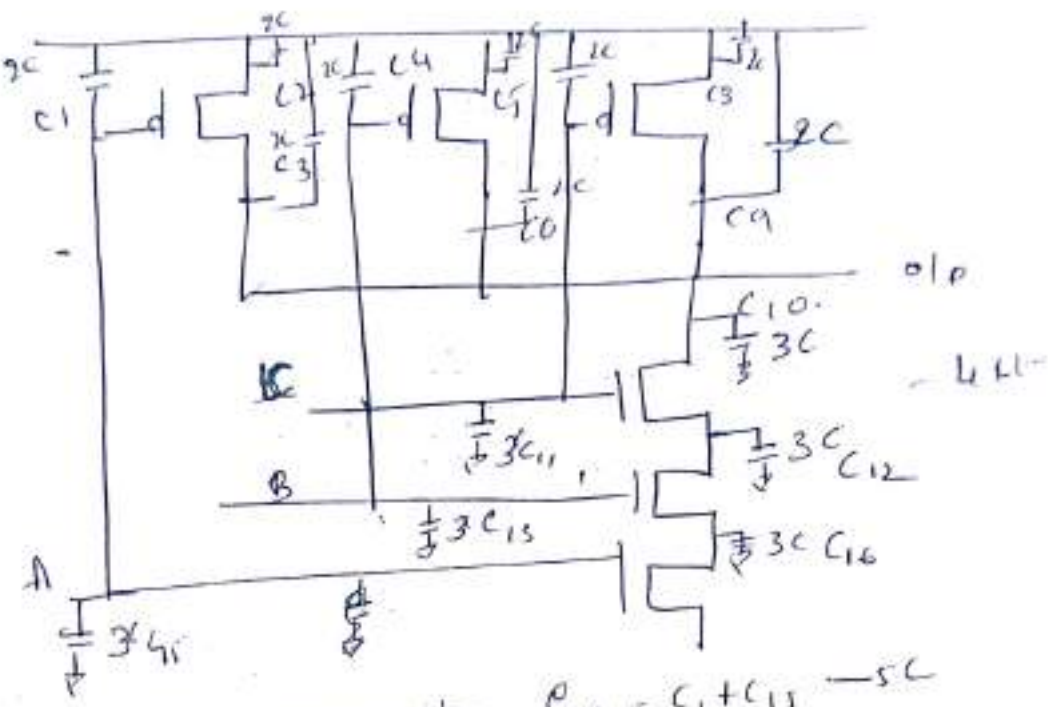
$C_{in} = 3$.

$g = 3/3$.

(8)

4b

3 i/p Nand gate with Capacitance



Capacitance → Gate

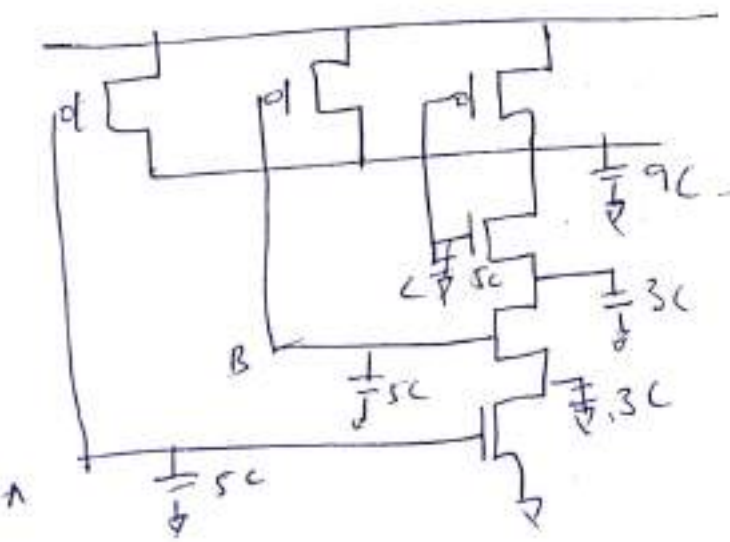
$C_{gA} = C_1 + C_{11} - 5C$

$C_{gB} = C_4 + C_{13} - 5C$

$C_{gC} = C_7 + C_{11} - 5C.$

o/p terminal

$\rightarrow C_3 + C_6 + C_9 + C_{10} = 9C$



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Department of Electronics and Communication Engineering

Internal Assessment Test-I Odd Sem AY 2021-22

Course Name: **CMOSVLSI DESIGN** Course Code: **15/17TE73** Date: 19/11/2021

Semester & Section: 7 D Max marks: 30 Time: 10.00 AM TO 11.00 AM

Note: Answer any Two full questions, choosing only One full question from each Module. Each full question carry maximum of 15 marks

Q N0		Module-1 Questions	MARKS	CO	RBTL
1	a	Explain Bi-CMOS fabrication in an n-well process	5M	2	L1
	b	Explain ideal VI characteristics of MOS transistor. Reduce expression of Ids.	10M	1	L1
		OR			
2	a	Design 3 i/p NOR Gate and Nand gate using CMOS logic	8M	1	L1
	b	Design the combinational logic circuit for y=(AB+CD)	7M	1	L1
		Module-2 Questions			
3	a	Explain different steps in CMOS fabrication Process	10M	2	L1
	b	Explain steps involved in VLSI Design flow	5M	1	L1
		OR			
4	a	Write a note on DC transfer characteristics of CMOS transistor	10M	1	L1
	b	Explain MOS Theory with neat diagram	5M	1	L1

Name & Signature of Course Instructor

18/11/2021

Scrutinized by (Name & Signature)

1) 19/11/2021 (Dr. JPP)
2) 19/11/21 (Dr. JNM)
3) HOD- 19/11/21

Kumbalagodu, Mysore road, Bangalore -74

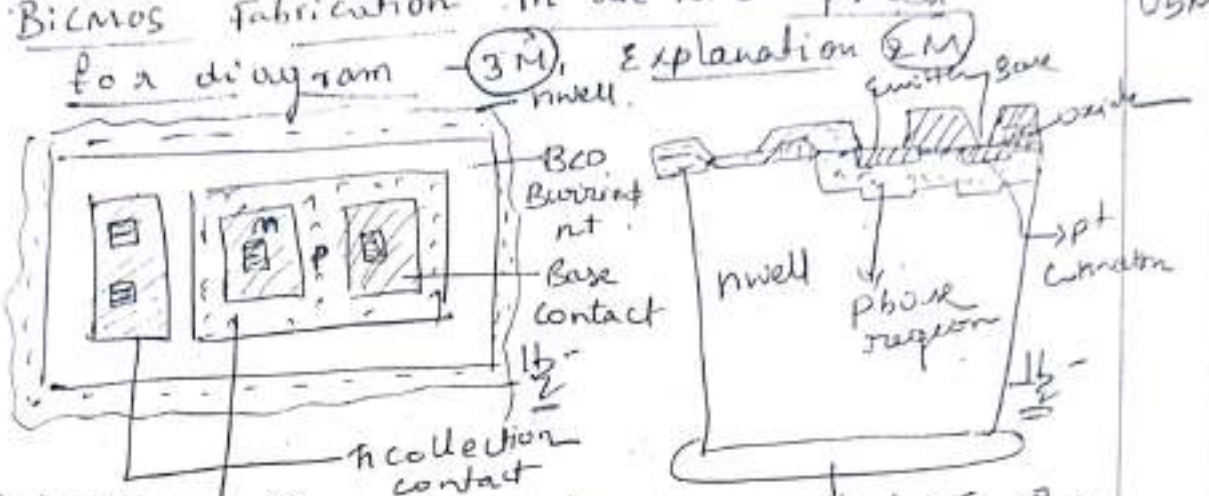
Department Of Electronics and Communication Engineering

Internal Assessment November 2021

SCHEME OF EVALUATION

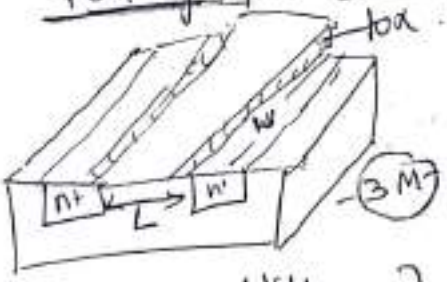
Subject: 17TE72 Semester VII
Sub Code: CMOS VLSI design Max Marks: 30
Faculty Name: Bhavya A.B

Q. No	SCHEME & SOLUTION	Marks
1a	BiCMOS fabrication in an nwell process. for diagram – 3M, Explanation 2M	05M



Explanation :-
(1) Bipolar transistor :- are npn & pnp, which have 3 terminals Emitter base collector (2M)
(2) two additional layer are aided (1) nT subcollector (2) pt & as layer.

1b.	VI characteristic MOS transistor Ids expression for graph – 2M, diagram – 3M, derivation-5M- & condition	10M



$$Ids = \frac{Q}{L/V} \quad -(1)$$

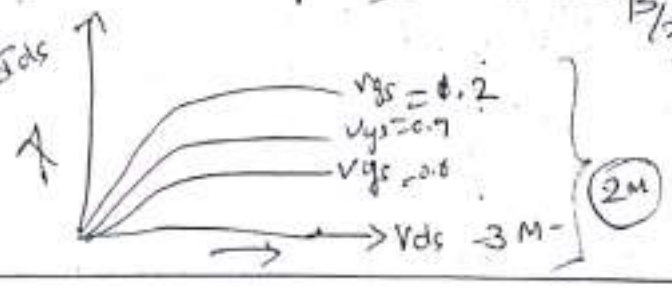
$$Ids = \mu_{Cox} \frac{W}{L} \left[V_{gs} - V_{th} - \frac{Vds}{2} \right] Vds \quad -(1)$$

$$Ids = \beta \left[(V_{gs} - V_t) - \frac{Vds}{2} \right) Vds \quad -(1)$$

cut off $V_{gs} < V_{th}$
Linear $V_{ds} > V_{gs} - V_{th}$
Saturation $V_{ds} > V_{gs} - V_{th}$ } -(1)M-

$$Ids = \begin{cases} 0 & V_g < V_{th} \\ \beta (V_{gs} - V_t - V_{ds}/2) V_{ds} & V_{ds} < V_{sat} \\ \beta/2 (V_{gs} - V_t)^2 & V_{ds} > V_{sat} \end{cases} \quad -(1)-$$

derivation + condition

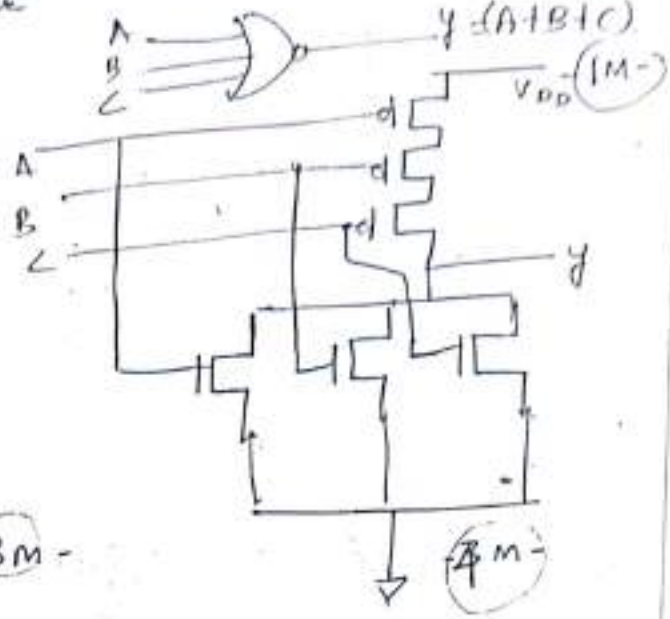


2a. 3 i/p NOR gate — 8M.

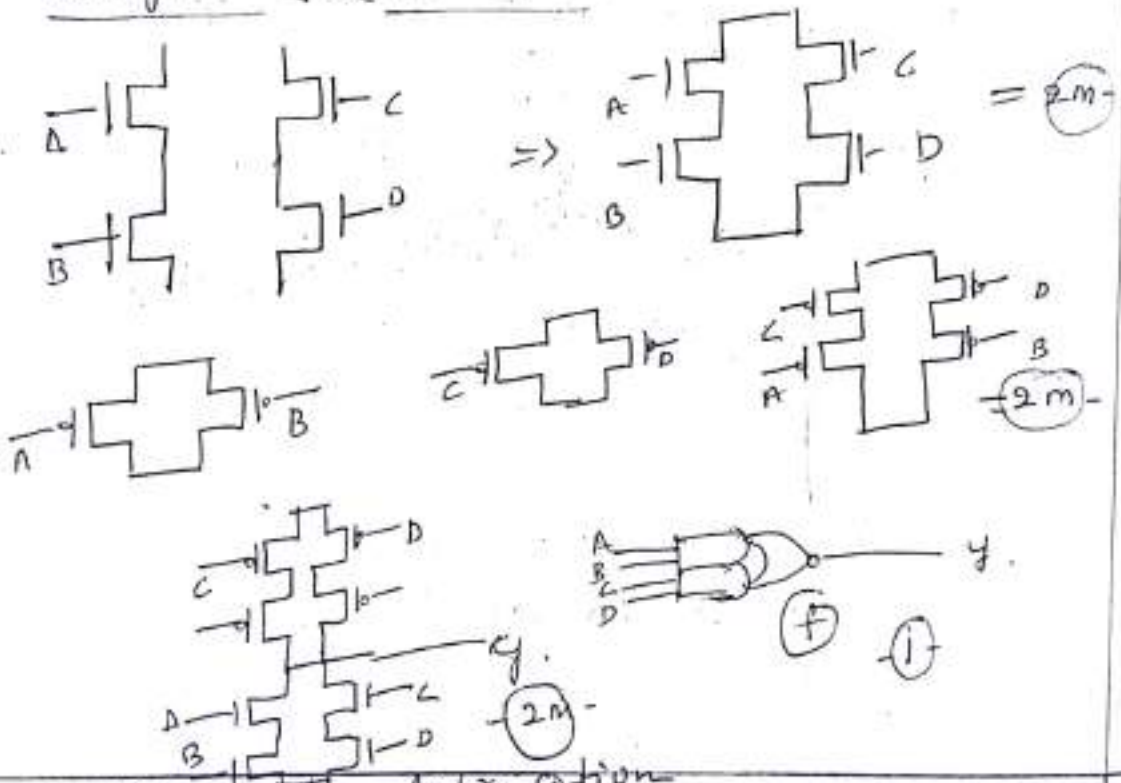
NOR gate

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

(3M)



2b. Design $Y=(\overline{AB+CD})$ — 7M



3a. Steps in fabrication — 10M

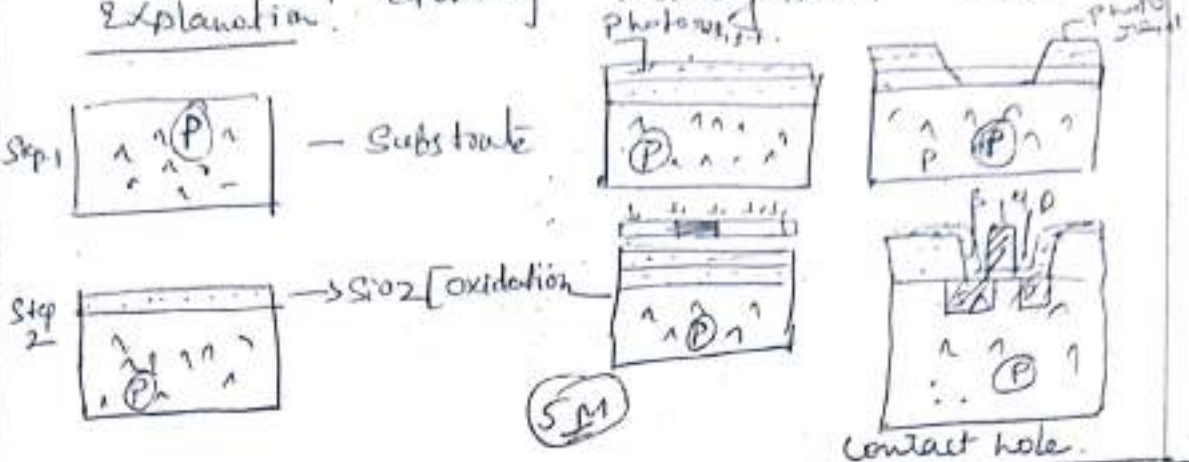
For fabrication steps — 05M

for diagram & Explanation — 05M

(1) wafer formation through CZochralski method
(2) Photolithography: positive photolithography, negative photolithography (5M)
(3) Well & channel formation: Epitaxy, deposition, Ion Implantation
(4) Isolation: shallow trench isolation, Isolation,
(5) Gate/src/drain/ formation
(6) metallization & contact: - evaporation, Sputtering, Anti

Steps: Doping, Oxidation, Lithography, Diffusion, Etching, Metalization. — 05 M

Explanation:



3b. Ates VLSI design flow

Design specification ⇒ i/p & o/p specification

① Schematic ② HDL Entry → Design Entry → Component are invoked, Interconnection done b/w component, Naming i/p & o/p

Functional Simulation / logical verification — 5M — logical error, Human error, Syntax error → Design entry

Functionally correct → logical & syntax correction

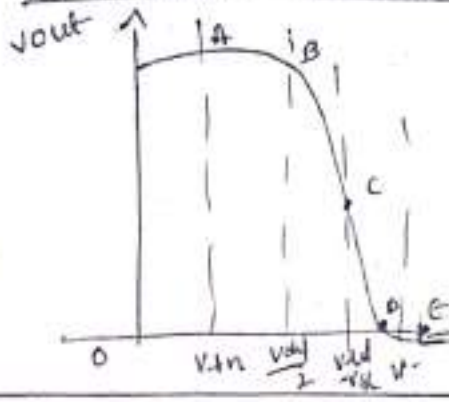
Planning & placement → Routing — Partitioning, placement, floor planning — 5M

Design routed

Timing Simulation → timing Analysis

Fabrication into chip → chip fabrication

4a. DC transfer characteristic — 10M



3M

graph — 3M

Condition — 4M

Explanation — 3M

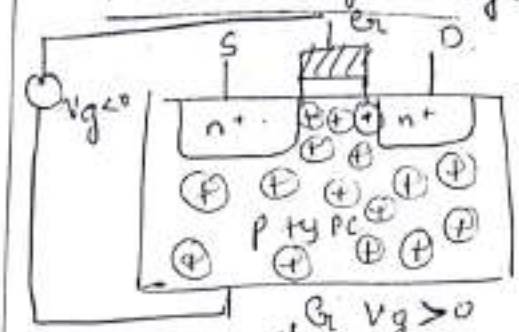
A → linear, C → Saturation
B → Saturation D → cut off

Region	Condition	PMOS	NMOS	O/P
A	$0 \le V_{in} \le V_{tn}$	linear	cut-off	$V_o = \frac{V_{dd}}{2}$
B	$V_{in} > V_{tn}$ & $V_{in} < \frac{V_{dd}}{2}$	Sat	linear	$V_o < \frac{V_{dd}}{2}$
C	$V_{in} = \frac{V_{dd}}{2}$	Sat	Sat	V_{out} ↓
D	$\frac{V_{dd}}{2} < V_{in} < \left\|\frac{V_{dd}}{2} - V_{tn}\right\|$	lin	Sat	$V_o > \frac{V_{dd}}{2}$
E	$V_{in} > V_{dd} - \left\|V_{tp}\right\|$	Cutoff	lin	$V_o = 0$.

4M

Types are:- ① CMOS complementary Inverter DC characteristic
② Beta ratio Effect. (1) $\beta_p/\beta_n > 1$ → Hi skew (2) $\frac{\beta_n}{\beta_p} < 1$ low skew
③ Noise margin $NM_H = (V_{OH} - V_{IH})$, $NM_L = (V_{IL} - V_{OL})$ 2M
④ Rational inverter transfer function ⑤ Pseudo transistor
⑥ Tristate inverter

4b. MOS theory. $V_g \geq 0$

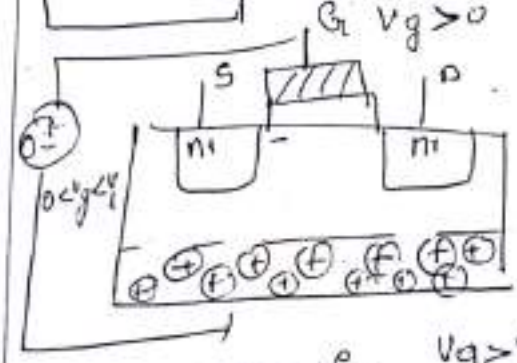


Accumulation region

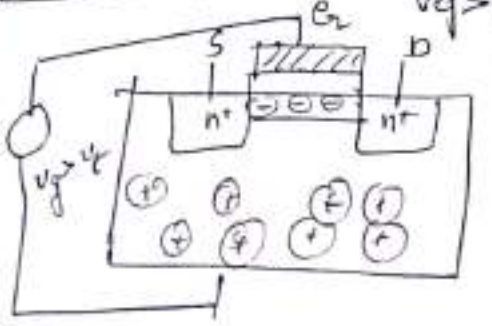
Form diagram 3M

Explanation 1M

Condition 1M



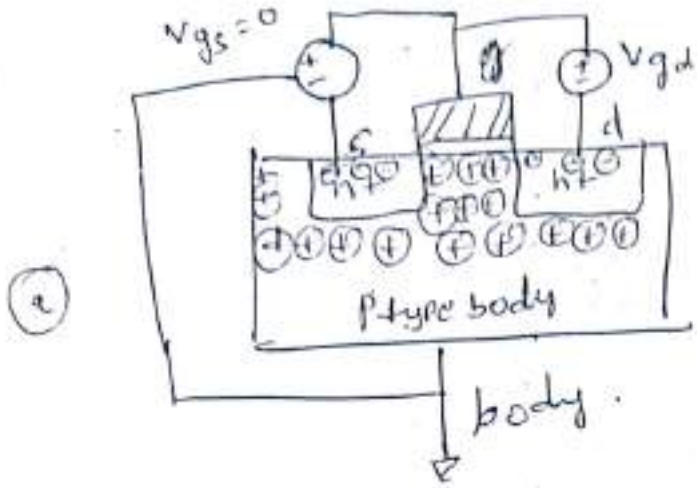
Depletion region



Inversion layer

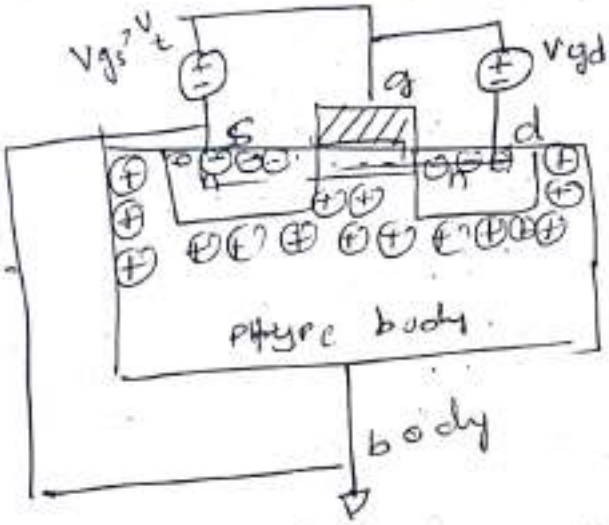
Condition
cutoff → $V_g < 0$
Linear $V_{gs} > V_{th}$
Saturation $V_{gs} \geq V_{th}$

i/p condition ½M



(a)

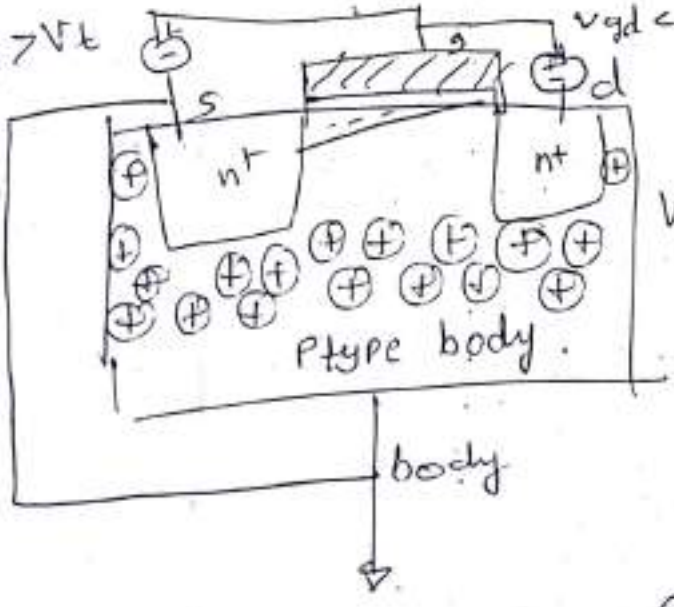
cutoff
No channel
$I_{ds} = 0$.



(b)

$0 < V_{ds} < V_{gs} - V_t$

Linear channel formed
I_{ds} Increases with V_{ds}.



(c)

$V_{ds} > V_{gs} - V_t$

Saturation
Channel pinch off
I_{ds} independent of V_{ds}.

fig: NMOS transistor demonstrating cutoff, linear & saturation.

O/P condition

for Linear → $V_{ds} < V_{gs} - V_{th}$

Saturation → $V_{ds} > V_{gs} - V_{th}$. ½m-

5M

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Department of Electronics and Communication Engineering

Internal Assessment Test-II Odd Sem AY 2021-22

Course Name: **CMOSVLSI DESIGN** Course Code: **15/17TE73** Date: 21/12/2021

Semester & Section: 7 D Max marks: 30 Time: 10.00 AM TO 11.00 AM

Note: Answer any Two full questions, choosing only One full question from each Module.Each full question carry maximum of 15 marks

QN0		Module-3 Questions	MARKS	CO	RBTL
1	a	Explain in detail about enhancement mode n-type transistor	5M	3	L1
	b	Explain the different types of contacts available in NMOS and CMOS logic along with lambda based design rules.	10M	2	L1
		OR			
2	a	Draw the stick diagram & layout for Y= AB+CD using CMOS technology.	8M	2	L1
	b	Explain BiCMOS deriver along with the mathematical	7M	2	L1
		Module-4 Questions			
3	a	Derive expressions for rise time and fall time of a CMOS inverter	10M	2	L1
	b	Express the different device parameters w.r.t scaling factors Ag,C0x,Cg,Qon,Ron	5M	2	L1
		OR			
4	a	Mention the types of Scaling models and Explain in detail about constant field scaling	10M	2	L1
	b	Illustrate the design process and approaches at different stages of design process	5M	3	L1

Name & Signature of Course Instructor

17/12/2021

Scrutinized by (Name & Signature)

1) Dr. APP 17/12/2021
2) Mr. CNS 18/12/21
3) HOD- 17-12-21

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Department Of Electronics and Communication Engineering

Internal Assessment Test – 1 / 2 / 3

SCHEME OF EVALUATION

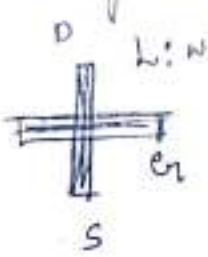
Name of The Course: CMOS VLSI design Course Code: 15/17EC73 Semester: VII

Max Marks: 30 Faculty Name: Bhavya A.B Date: 17/12/2021

Q.No	SCHEME & SOLUTION	Marks

(1) Enhancement mode n-type transistor

Diagram



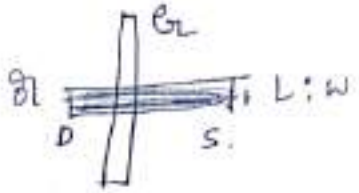
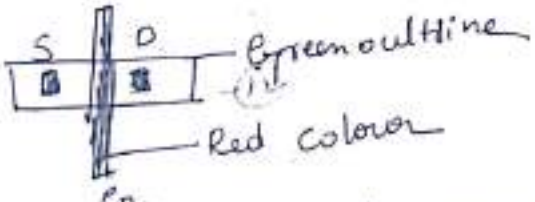
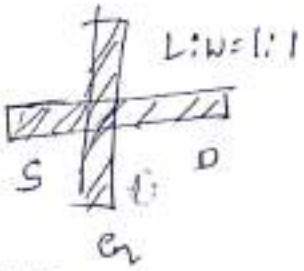


Diagram (2M)





N type Enhancement mode transistor

Explanation (2M)

Comments

(1) Enhancement mode is a type of transistor in which channel is present in the transistor

(2) The manufacturer provides channel in which the transistor will be working at $V_{gs} > V_{th}$.

(3) It will be have 2 region of operation
(1) Linear region (2) Saturation region.

(4) Different types of contact available in NMOS & CMOS logic with λ based λ based design rules.

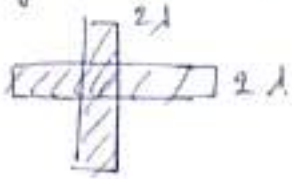
Explanation (3M)

(1) N diffusion – 2λ
(2) P diffusion – 2λ
(3) n.diff/p.diff to diffusion – 3λ
(4) Pdiff / ndiff → 1λ
polysilicon – 2λ

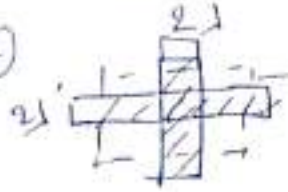
polysilicon

Q. No	SCHEME & SOLUTION	Marks

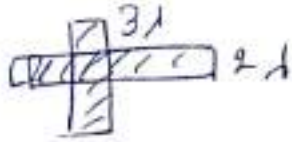
Diagram Coorries (8 M)

① 

→ NMOS Enhancement transistor 1
2λ x 2λ Dimension

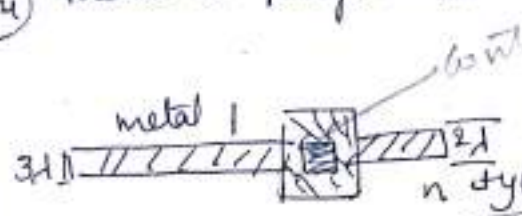
② 

6λ x 6λ Implant 1
→ 2λ x 2λ NMOS depletion

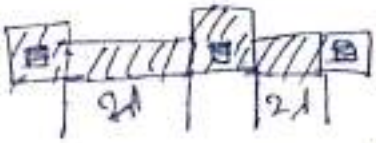
③ 

2λ x 2λ PMOS Enhancement 1

④ Metal to polysilicon & metal to depletion

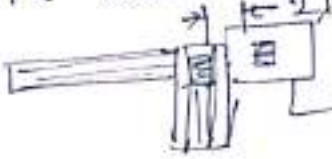


⑤ Min Seperation b/w multiple cuts.

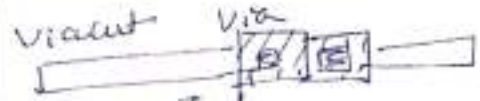


1

⑥ Via Contact from metal 2 to metal 1



minimum seperation
4λ x 4λ area of overlap with 2λ x 2λ Via a center 1



1
used to contact M2 to diffusion

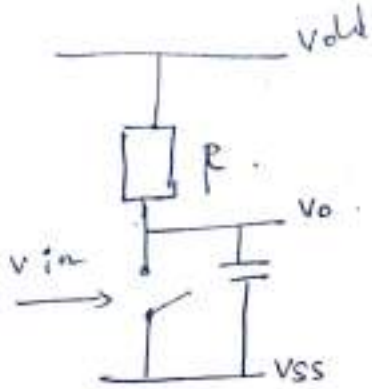
⑦ Contact polysilicon to diffusion

1

Q. No	SCHEME & SOLUTION	Marks

2(b) BiCMOS driver. Along with mathematical expression. | 7M

BiCMOS driver



(2M)

Explanation (1M)

(*) The BiCMOS driver can be operated with much smaller i/p voltage swing than MOS transistor, & still switch relatively large current.

(2M)

delay $\Delta t = \frac{C_L}{g_m}$ ——— (1) (1M)

Wherein g_m – device trans conductance

Id is relatively high g_m.

Δt – Small.

2 main components T_{in} & T_L.

T_{in} -> Initial time necessary to charge the Base emitter junction Bipolar transistor

T_L -> time taken to charge the o/p load capacitance C_L.

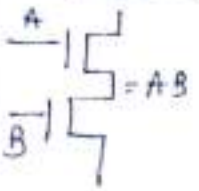
$$T = T_{in} + V/I_d (1/h_{fc}) C_L \quad \text{——— (2)} \quad (1M)$$

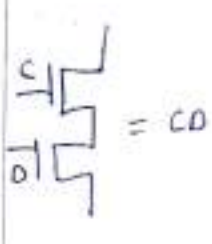
where h_{fc} – transistor current gain

T_{in} -> time to charge up base / emitter junction.

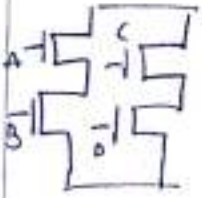
(2) a $\overline{Q} = \overline{AB + CD}$ using CMOS logic.

NMOS

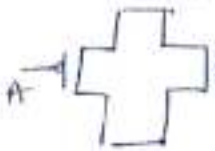




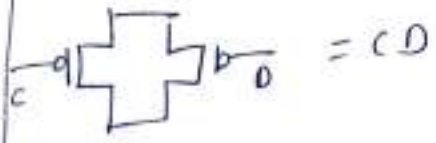
AB + CD



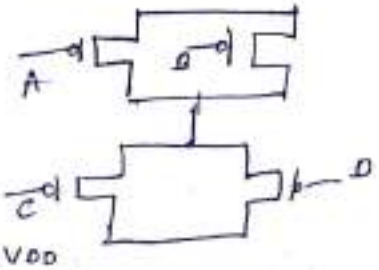
PMOS



(1M)

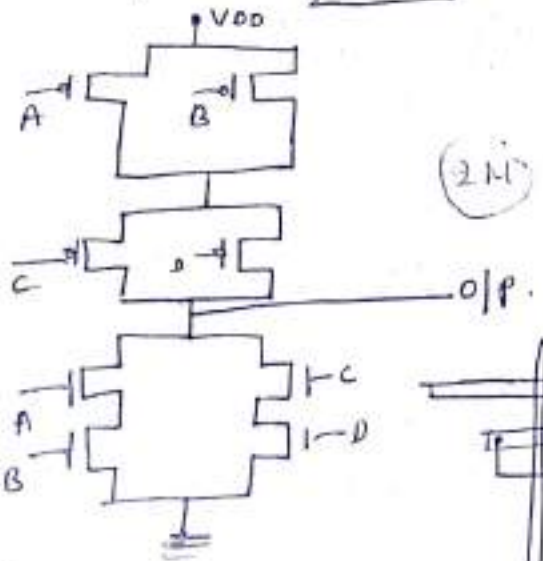


AB + CD

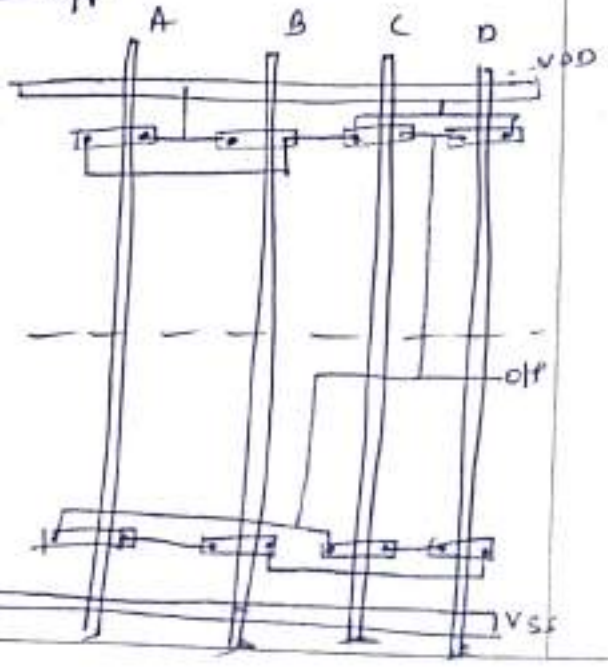


(1M)

AB + CD



(2M)



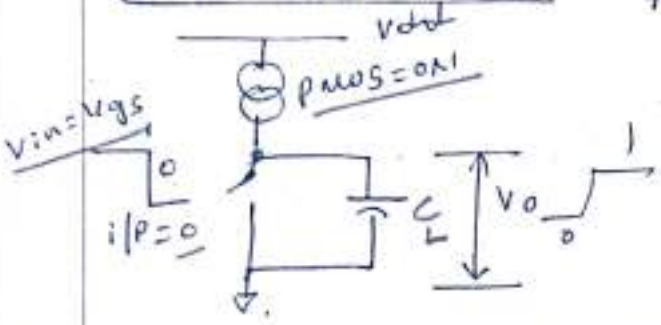
Stick diagram

(4)

Q. No	SCHEME & SOLUTION	Marks
7(a)	Expression for Rise & fall time derivation.	10 M

Rise time Estimation

PMOS Stays in Saturation for Entire charging of C_L



-1M-

Saturation current Expression

$$I_{dsp} = \frac{\beta_p (V_{gs} - |V_{tp}|)^2}{2} \quad \text{——(1)} \quad -1-$$

$V_o = I_{ds} \cdot R_s$ $\qquad V_o = I_{ds} R_s$.

$$V_o = \left(\frac{I_{ds} \cdot t}{C_L}\right) \text{——(3)} \qquad \boxed{\tau = R_s C_L}$$

$$R_s = \tau / C_L = \frac{t}{C_L} \text{——(2)} \quad -1- \qquad V = IR, \quad V = \frac{I_{ds} \cdot t}{C_L}$$

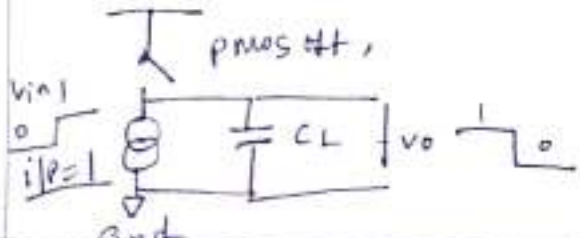
$$V_o = \frac{\beta_p (V_{gs} - |V_{tp}|)^2 t}{2C_L} \quad -1-$$

$$\boxed{t = \frac{2 C_L V_o}{\beta_p (V_{gs} - |V_{tp}|)^2}}$$

$\therefore t = t_r$ (rise time), When $V_o = V_{dd}$, $V_{gs} = V_{dd}$ at Saturation, $V_{tp} = 0.2 V_{dd}$, then

$$\tau_r = \frac{2 V_{dd} C_L}{(0.8 V_{dd})^2 \beta_p} = \boxed{\frac{3.125 C_L}{\beta_p V_{dd}}}$$

$$\boxed{\tau_r = \frac{3 C_L}{\beta_p V_{dd}}} \text{——(A)}$$



-1 M-

$I_{dsn} = \frac{\beta_n (V_{gs} - V_{tn})^2}{2}$ -1

$V_{out} = \frac{I_{dsn}}{C_L} = \frac{\beta_n (V_{gs} - V_{tn})^2}{2} \times \frac{t}{C_L}$ -1

$t = \frac{2 C_L V_o}{\beta_n (V_{gs} - V_{tn})^2}$ -1

When $V_o = V_{dd}$, $t = \tau_p$, $V_{gs} = V_{dd}$, $V_{tn} = 0.2 V_{dd}$

$\tau_f = \frac{3 C_L}{\beta_n V_{dd}}$ -1

$\frac{\tau_r}{\tau_f} = \frac{\frac{3 C_L}{\beta_p V_{dd}}}{\frac{3 C_L}{\beta_n V_{dd}}} = \frac{\beta_n}{\beta_p}$ -1

3(b) Expression for A, C_{ox}, C_g, Q_{on}, R_{on}. (5M)

(i) Area $A = L \times W$.

L & W are scaled by $1/\alpha$.

$\therefore$ A is scaled by $1/\alpha^2$. -1

(ii) C_{ox} → gate capacitance / unit area.

$C_{ox} = \frac{\varepsilon_{ox}}{D}$ $\varepsilon_{ox} = \varepsilon_{ins} \varepsilon_o$ (constant)

$D = 1/\beta$.

$C_o = \frac{1}{1/\beta} = \beta$ -1

(iii) $C_g = C_o \cdot L \cdot W$. → C_g (gate capacitance)

$= \beta \cdot 1/\alpha \cdot 1/\alpha = \beta/\alpha^2$ -1

Parasitic capacitance C_x

Carrier density in channel Q_{on}

$Q_{on} = C_o V_{gs} = \beta \times \frac{1}{\beta} = 1$ -1

R_{on} = channel resistance $R_{on} = k_N \cdot \frac{1}{Q_{on} W}$

Q No	SCHEME & SOLUTION	Marks

$R_{on} = \frac{1/\alpha \cdot}{1/\alpha} \times 1 = 1$. μ -> constant

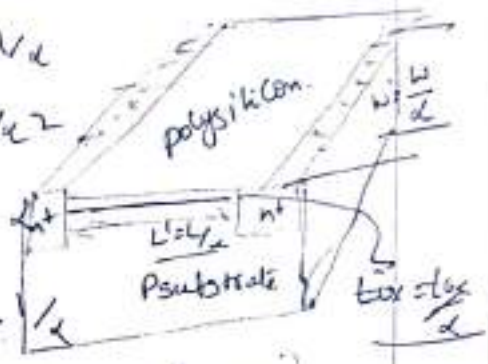
$g_{on} = 1$

4(a) Constant field Scaling

constant E table

Parameter

- V_{DD} - Supply voltage — $1/\alpha$
- L - channel length — $1/\alpha$
- W - channel width — $1/\alpha$
- D - Gate oxide thickness — $1/\alpha$
- A_g - Gate area — $1/\alpha^2$
- C_{ox} - Gate C per unit area — α
- C_x - parasitic capacitance — $1/\alpha$
- g_{on} - carrier density — 1
- R_{on} - Channel resistance — 1
- I_{ds} - saturation current — $1/\alpha$
- A_c - conductor area — $1/\alpha^2$
- I - current density — α
- V_{of} - logic level — $1/\alpha$
- E_g - Switching Energy — $1/\alpha^3$
- P_g - power dissipation per gate — $1/\alpha^2$
- N - Gate / unit area — α^2
- P_a - power dissipation / unit gate area — 1
- T_d - Gate delay — α
- f_o - max operation freq. — $1/\alpha$



(a) $\times 1/\alpha$
(b) $\times 1/\alpha$

Doping Acceptor Concentration

2M

Explanation

(a) Each dimension will be scaled down along with the L, W, t_{ox}, x_j, V_{dd}, I_s in constant field scaling.

4 (b) Stages of Design process :-

Design process stages are follows.

1. Convention circuit Symbol
2. logic Symbol
3. mask Layouts
4. stick diagram
5. Architectural block diagram
6. floor plan
7. Any Combination of logic Symbol & stick diagram is convinient at a particular stages.

(1½)

(1½)

Process.

1. structural design.
2. functional division / subdivision
3. top down approach.
4. Coupling submodule interaction.
5. physical proximated.
6. Adaption to new process must occur in short time - time to market

(2½)

USN | 1 | D | B | | | | | | | |

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Department of Electronics and Communication Engineering

Internal Assessment Test-III Odd Sem AY 2021-22

29/01/2022

Course Name:**CMOSVLSI DESIGN** Course Code: **15/17TE73** Date: 28/01/2022

Semester & Section: 7 D Max marks: 30 Time: 10.00 AM TO 11.00 AM

Note: Answer any Two full questions, choosing only One full question from each Module.Each full question carry maximum of 15 marks

QNo		Module-3 Questions	MARKS	CO	RBTL
1	a	Explain 4×4 structure of a barrel shifter with a neat diagram.	5M	4	L2
	b	Implement an ALU function with an Adder	10M	3	L3
		OR			
2	a	Write a note on FPGA architecture	8M	3	L1
	b	Design a general 4 Bit adder	7M	4	L2
		Module-4 Questions			
3	a	Explain diagram of built in self-test with diagram	10M	5	L2
	b	Explain pseudo random sequence generator with diagram	5M	5	L1
		OR			
4	a	Explain the scan design techniques	10M	5	L2
	b	List out the manufacturing test principles	5M	5	L1

Name & Signature of Course Instructor

13/1/2022

Scrutinized by (Name & Signature)

1) DR. IPP 18/01/22
2) DR.C NS 13/1/22
3) HOD- 24.01.22

DON BOSCO INSTITUTE OF TECHNOLOGY

Kumbalagodu, Mysore road, Bangalore -74

Department Of Electronics and Communication Engineering

Internal Assessment November 2021

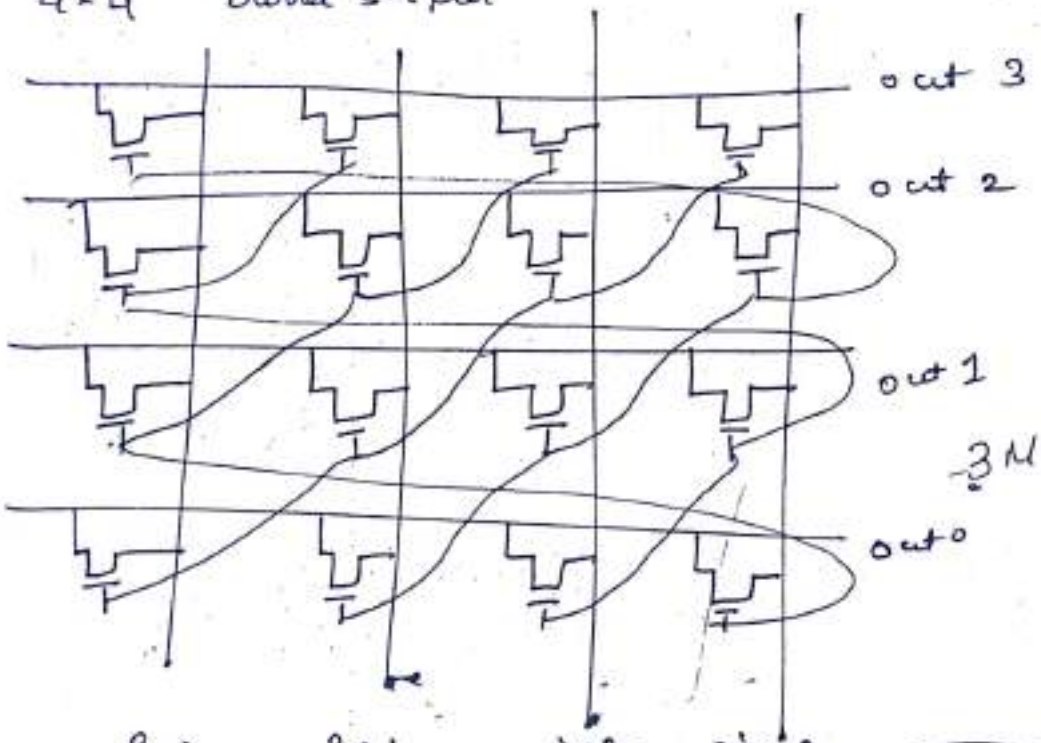
SCHEME OF EVALUATION

Subject: CMOS VLSI Design. Semester: 7th D.

Sub Code: 15|17 TE73 Max Marks: 30 M

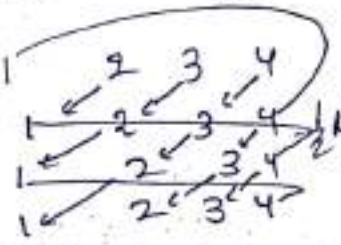
Faculty Name: Bhavya A.B

Q. No	SCHEME & SOLUTION	Marks
1 (a)	4×4 barrel shifter	5M



3M

1 2 3 4		½M
2 3 4 1		
3 4 1 2		
4 1 2 3		



½M ½M

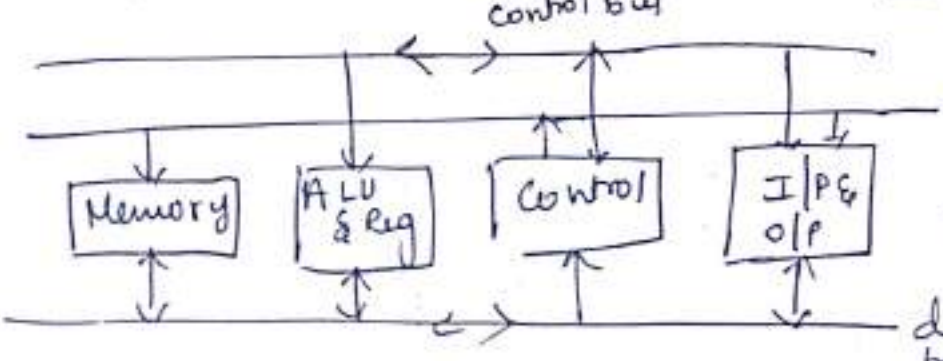
(1) 01100 11 → 11 01100

↳ right (2) 1M

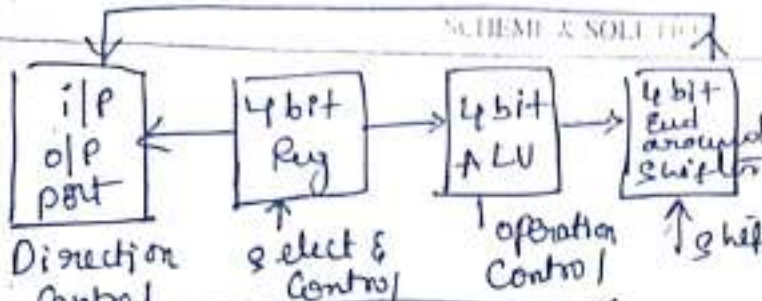
(2) 00 11011 ← 00 11011

Left by (3) 1M

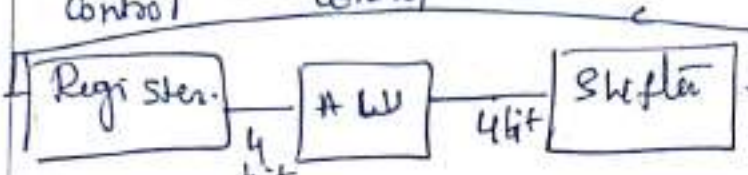
1 (b)	Implement ALU function with an Adder	10M



2M

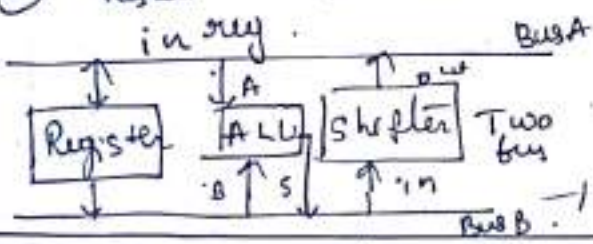


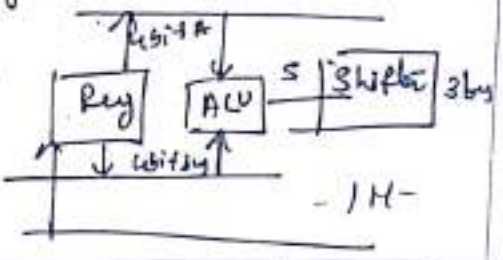
– 2M –



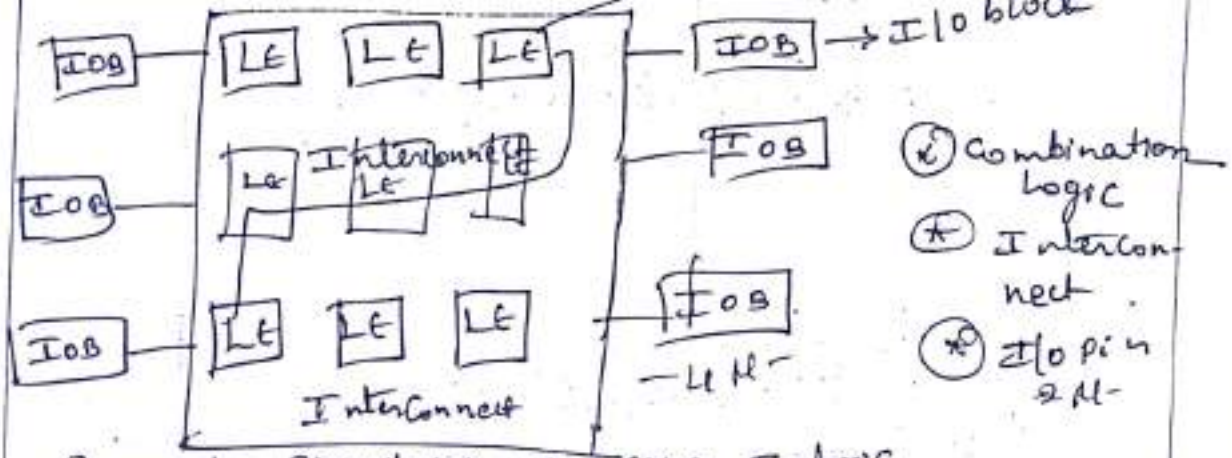
– 2M –

(a) 1st operation from Reg to ALU to stored
(b) 2nd operand —"— —"—
(c) operand are used with ALU operation & result is produced & stored in ALU. – 2M –
(d) Result is passed through shifter & Stored in reg.

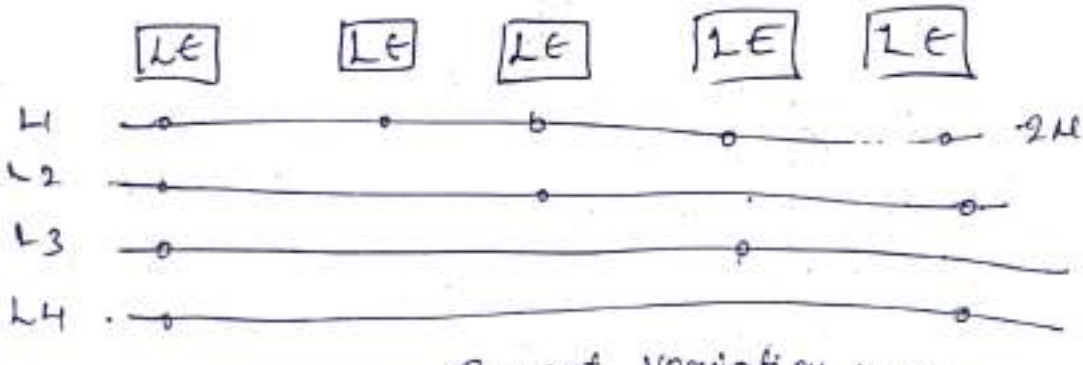




2a. FPGA architecture — 3M



General Structure of FPGA Fabric.



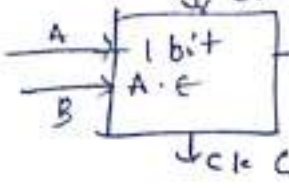
Segment variation length.

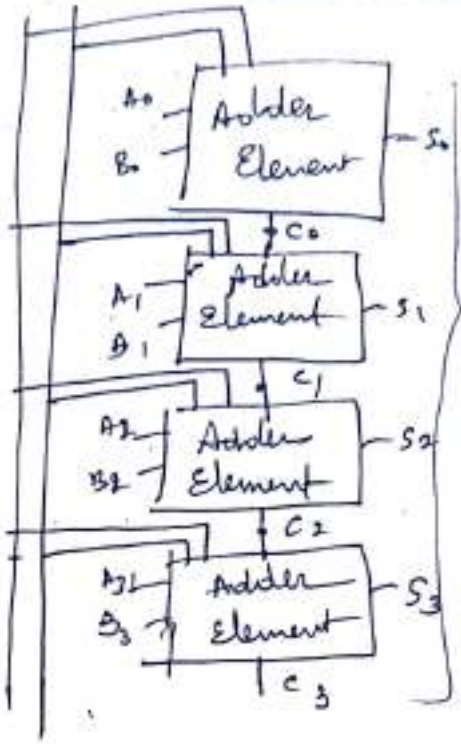
Q. No	SCHEME & SOLUTION	Marks

8b Adder 4 bit.

7M

Standard adder





a) 4bit we need to cascade 4 adder Element to produce

I/p → Sum of 4bit Size

→ Carry of 1-bit.

$S = \overline{H_K} C_{K-1} + H_K \overline{C_{K-1}}$

$C_K = A_K B_K + H_K C_{K-1}$

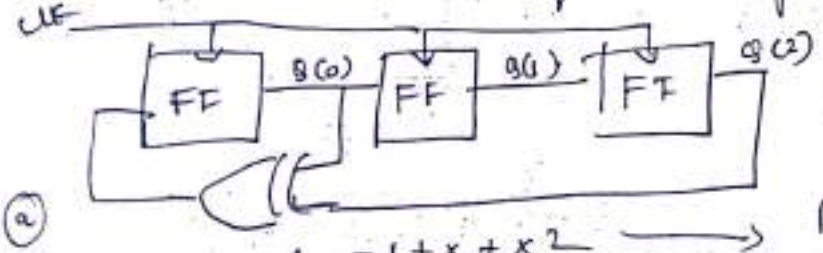
$H_K = A_K' B_K + A B_K'$

$C_K = AB + H C_{K-1}$

2-M-

5b Pseudo Random sequence generator

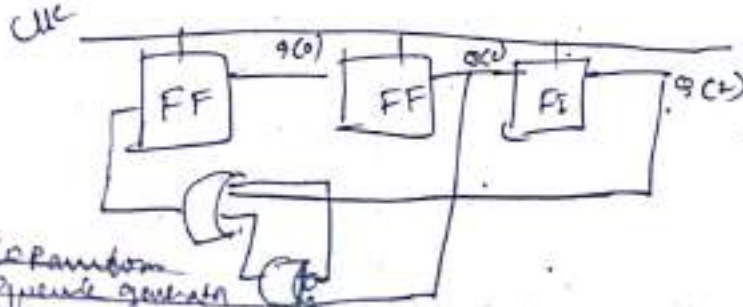
5M



— 2M —

(a) $f x = 1 + x + x^2$ → PRSG produce the polynomial function

-1M-



-2M-

Pseudo Random sequence generator

3 (a) PRBS is defined by polynomial of some Length n. It is constructed from LFSR.

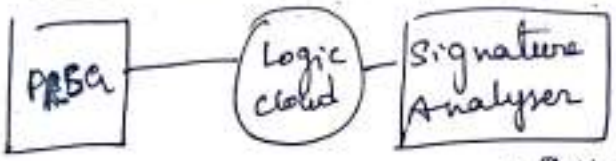
(b) LFSR made up of n Filpflop connected in series

(c) O/P of XOR fed back to i/p of LFSR.

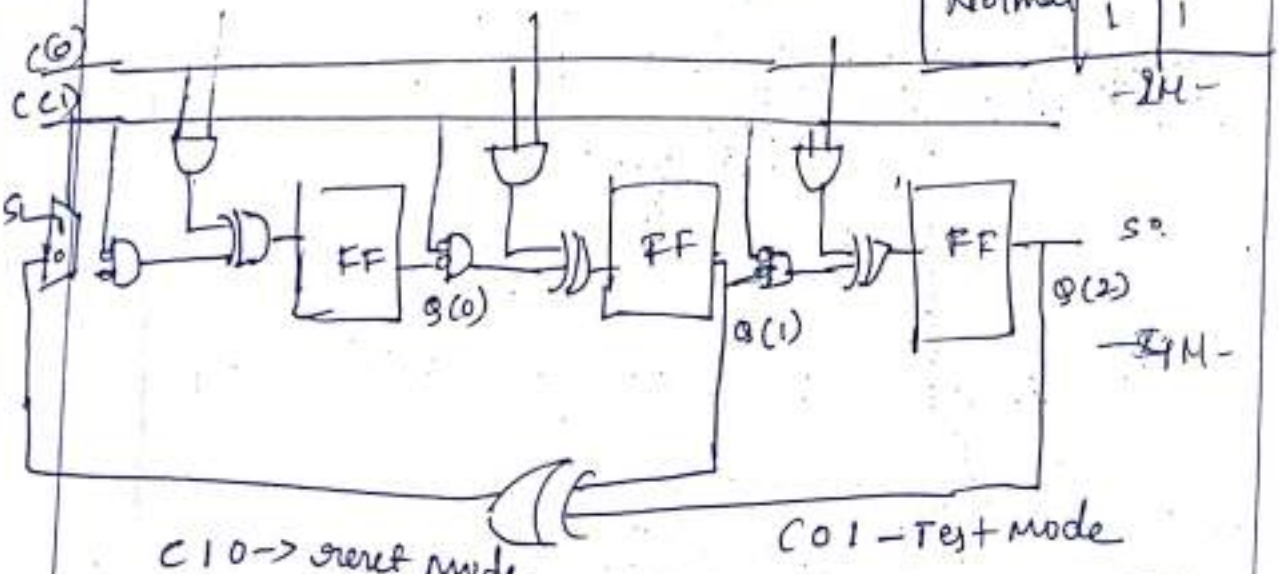
(d) N bit LFSR can be connected into n bit CFSR by adding n-1 i/p NOR gate

3a Built in self test BIST :-

Self checking design



Mode	C(1)	C(0)
Scan test	0	0
Reset	0	1
Normal	1	0
	1	1



C10 -> reset mode

C11 — Normal Mode

C01 - Test mode

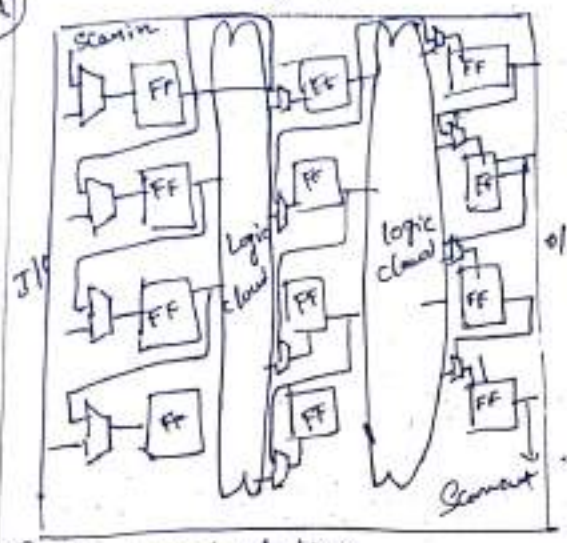
C00 — Scan Mode

There are the various comparision which provider package that support BST.

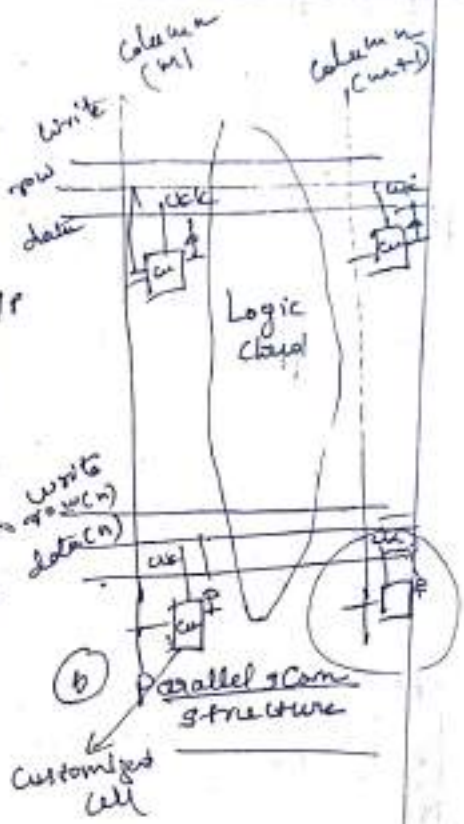
Q. No | SCHEME & SOLUTION | Marks

Scan based design

(a)



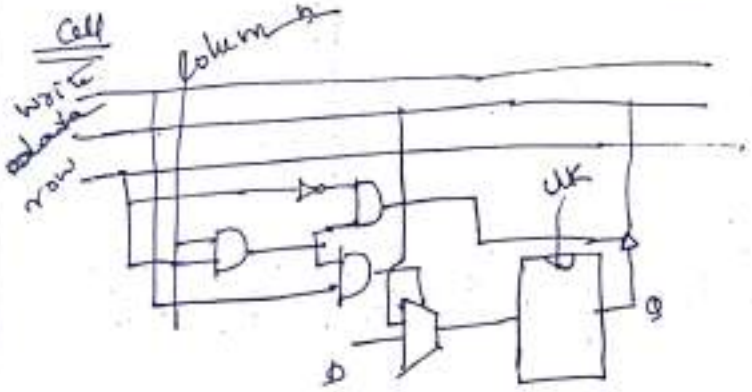
(a) Scan based testing



(b) Parallel scan structure

Customized cell

(b)



Customized cell

(a) Scan based design is a D F/F flop. Preceded by multiplexer

(b) mux are used to give many o/p.

(c) Serial scan area & delay of extra multiplier is more.

4(b) Manufacturing test principles

① Fault Model. -1M-

- Stuck-at fault
  - Stuck at 0's - VGND
  - Stuck at 1's - Vcc
  - ——— fault

Short circuit & open circuit fault.

② Observability :- Ability to determine the signal value at any node in a ckt by controlling the ckt i/p & o/p -1M-

③ controllability :- Ability to establish signal value at any node -1M-

④ fault coverage :- measure of goodness of a set of test vector -1M-

⑤ Automatic test pattern generator :- tools used for testing.

⑥ Delay fault testing :- Failure occurs in cmos affects the timing but not the functions. -1M-

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DB

BLUE BOOK

Name: VIKAS.T.N

USN: 1DB18EC157 Sl.No..... (for First year - Students only)

Subject: VLSI Design Subject Code: 18EC72

Branch: ECE Semester: 7th Section: C

Test No	Date	Max. Marks	Marks Obtained	Signature of the Faculty
I	18/11/2021	30	30	
II	20/12/2021	30	29	
III	27/01/2022	30	28	
I A Marks (Average of best two test marks)		40	29+10 = 39	

Signature of the Student

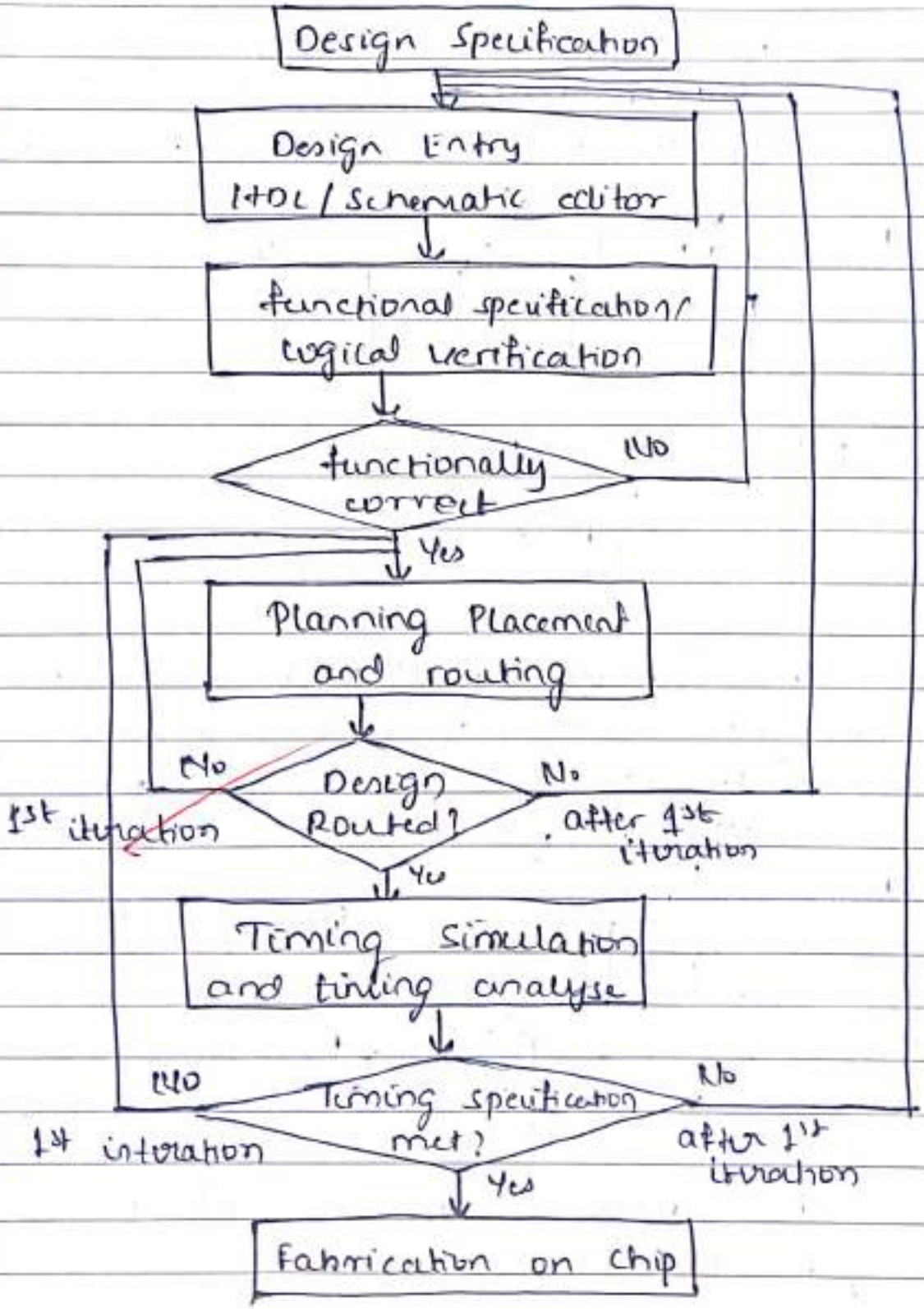
Signature of the Faculty

18/11/2021

I.A-01.

2.b.

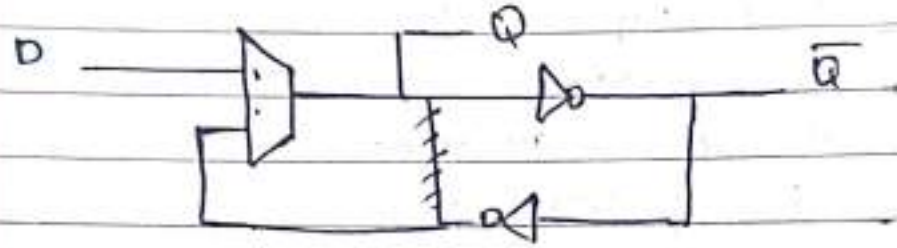
Steps involved in VLSI Design flow.



2a. Operation of D-latches and D-flipflop.

→ D-Latches

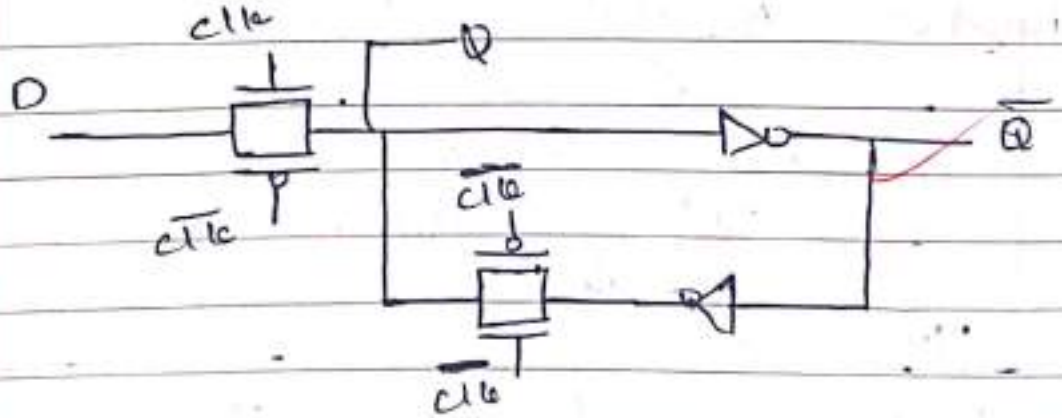
• The D-latches are designed using two input multiplexer and 2 inverter invoking in the circuit as shown below



T-T ⇒

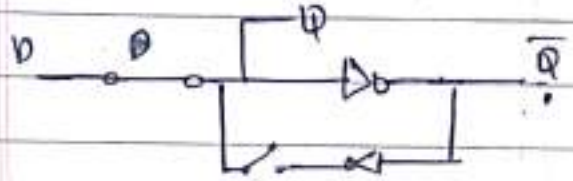
D	Q	$\overline{Q}$
0	0	1
1	1	0

The above multiplexer can be designed using two transmission gates and the ckt is like



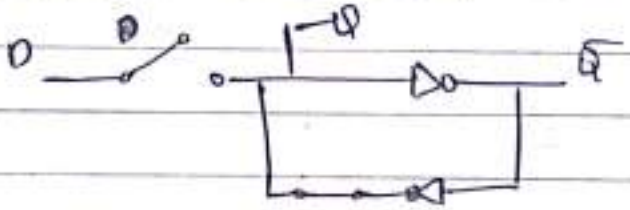
the above is the use of transmission gate to design multiplexer

• when clk = 1, the 1st transmission gate will turn ON and the output will be Q and it is same as D.
• when clk = 0, the 2nd transmission gate will turn ON and the previous value of D will be trapped inside

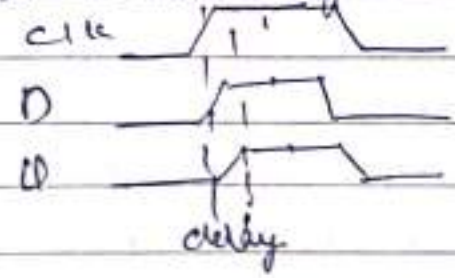


⇐ this is when clk = 1

⇒ when clk = 0 ⇒

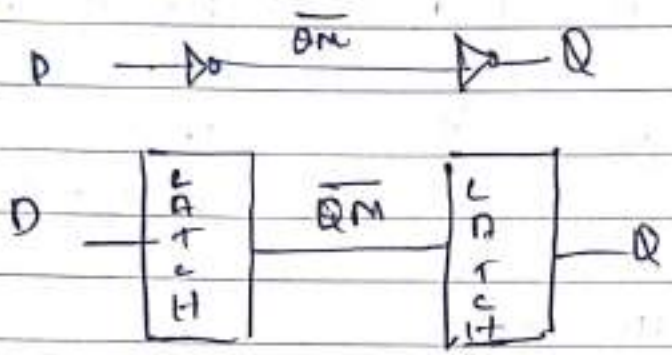


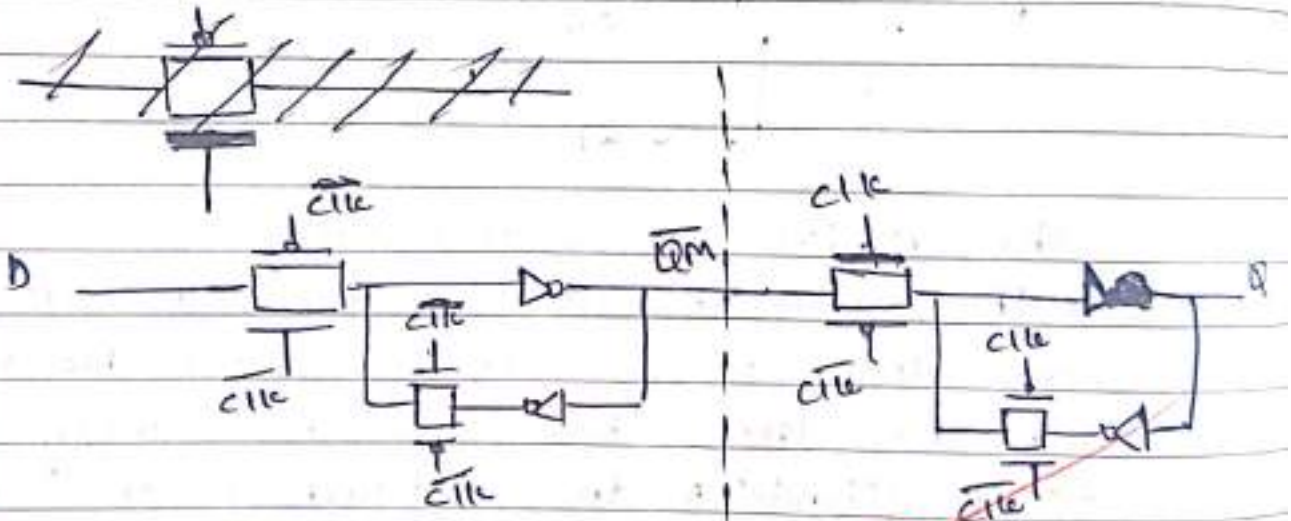
The D-latch is a level triggered and when the level is high the clk=1 and level is low the clk=0. Because of this there will be delay in the output with respect to the time or clk pulse. To overcome this is flipflop which is edge.



→ D-flipflop

• The d-flipflop is made up using two latches and using the two level triggered. it can be working on edge triggered.





Master
→ Negative-level sensitive

Slave
→ positive-level sensitive

• when clk = 0, the master g-side gets ON and it is negative-level sensitive and the value in D comes to $\overline{QM}$. and at next the value to trapped and in which be is there in the slave

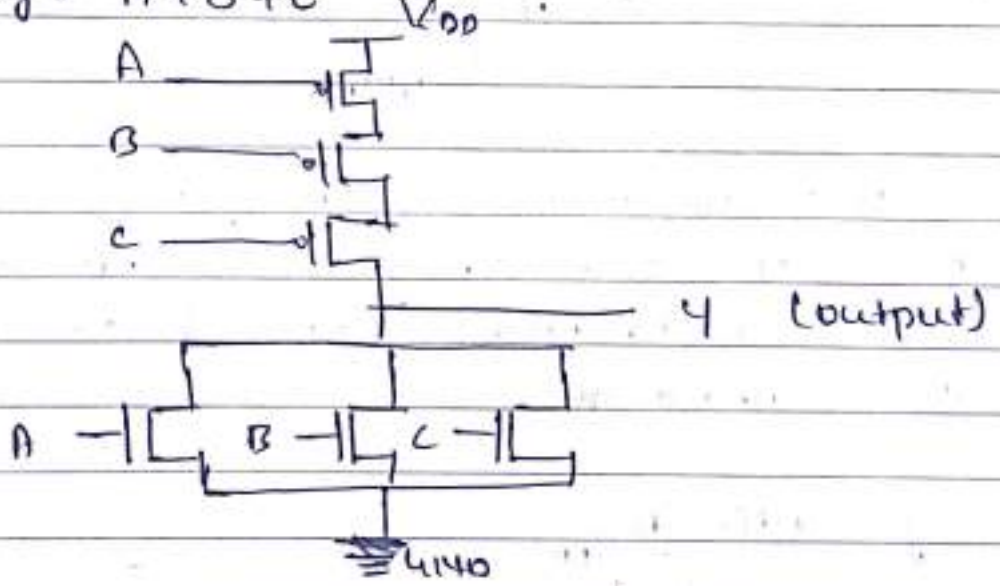
• when clk = 1, the slave part gets active and the value in $\overline{D}$ gets passed to Q and thus the movement from D to Q. this is positive-level sensitive.

→ Thus at ck as in latch there will no delay caused with respect clk pulse.

3.a.

• 3 i/p NOR Gate.

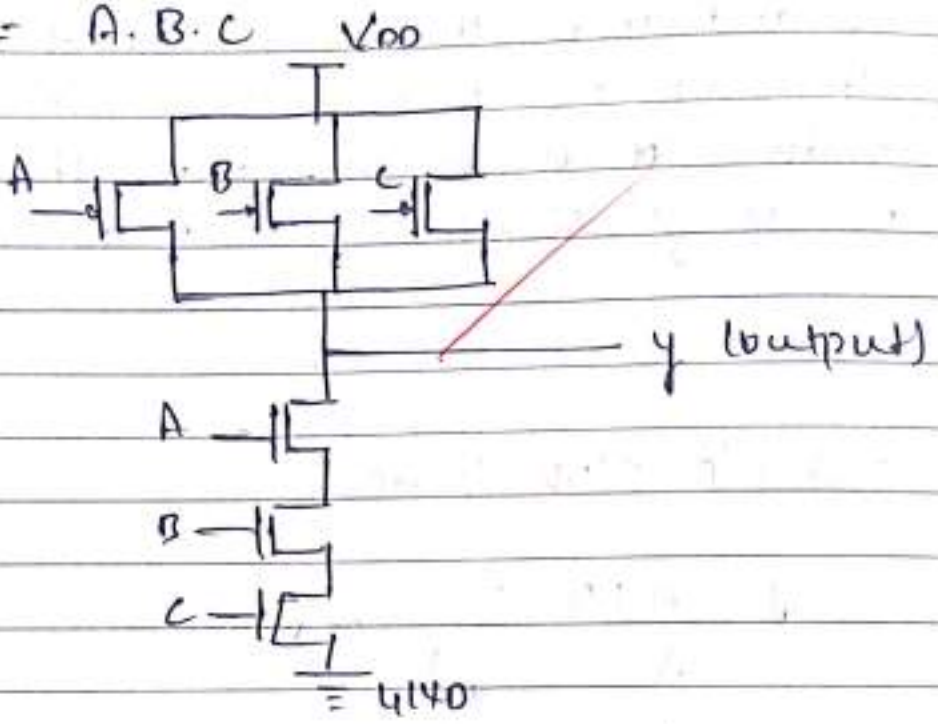
$Y = \overline{A+B+C}$



If the nMOS ~~transistor~~ is connected in parallel either of them can be high to get ON and in pMOS since it is series all the input should be low to turn all the pMOS.

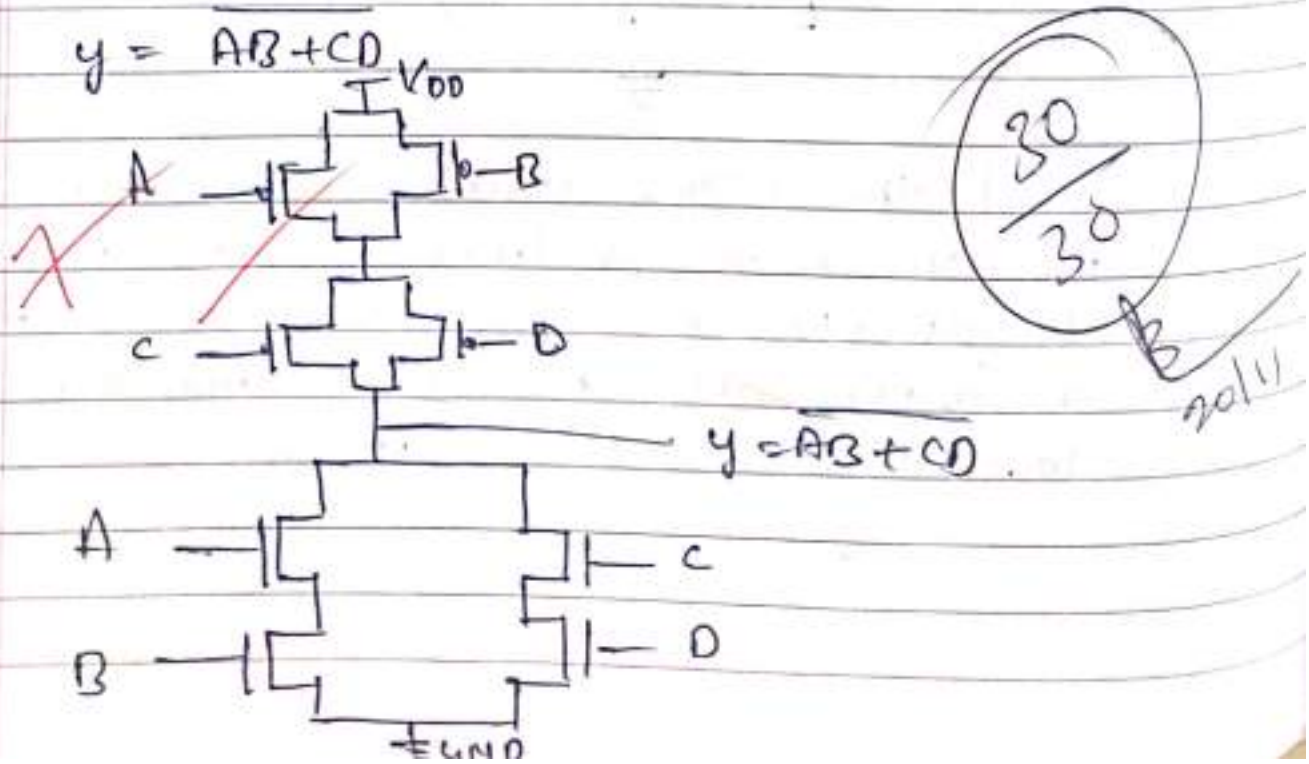
• 3 i/p NAND gate.

$y = \overline{A \cdot B \cdot C}$



• Here, to turn ON the nMOS, all should be ON since they are connected in series and in pMOS either 1 can be ON to connected to or turn ON.

3b. $y = \overline{AB+CD}$



30/30

2011

20/12/14
SGD

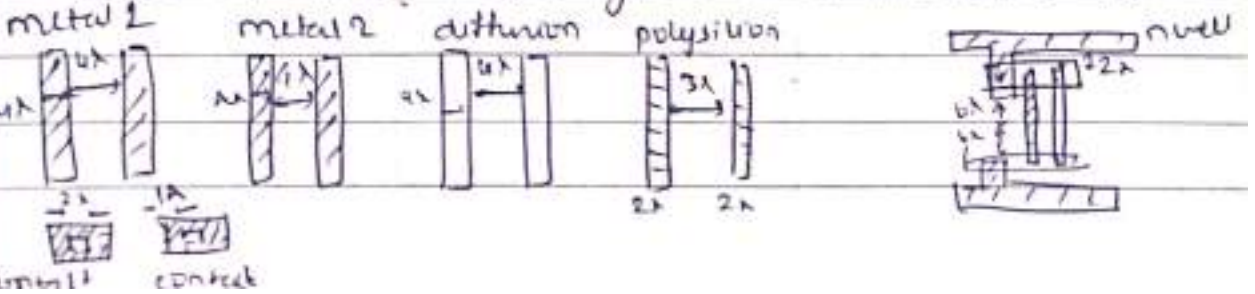
T.A-02

1b. Lambda based layout design rule:

- It is based on single parameter λ
- λ is the half of the draw transistor channel length
- where channel length is the distance between source and drain
- It is measured in always in microns and value should be above 0.1 Ohm

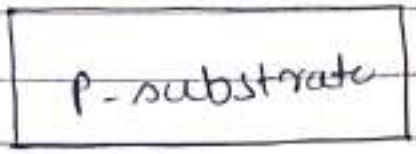
design rules

1. The metal and diffusion must have minimum width and spacing of 4λ
2. contacts are 2λ×2λ and the spe 1λ layer above and below
3. Polysilicon layer must be having width of 2λ
4. Polysilicon and contact must be spaced with 3λ with other polysilicon or contact
5. Polysilicon overlaps diffusion with 2λ where the transistor is desired and spacing of 1λ where there is no transistor desired
6. nwell is surrounded by pmos by 6λ and avoids the nmos by 6λ
7. pmos will be wider than nmos because the movement of holes is slower than electron and thus generates the current

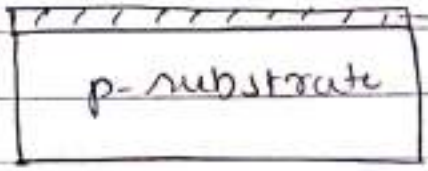


1a n-well CMOS fabrication process

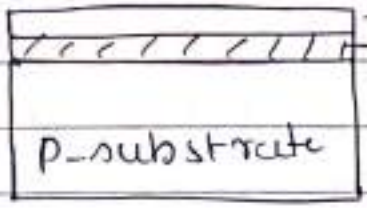
- Here we will be taking p-substrate and will be performing n-well fabrication



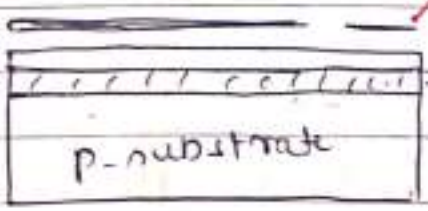
- Next we will be performing oxidation at nearly 900°C and deposit silicon oxide layer over substrate



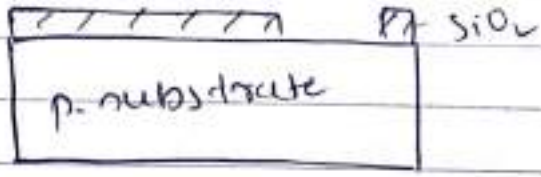
- Next photolithography layer process will be performed



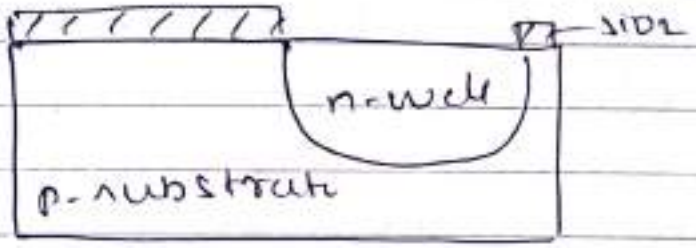
- The ~~window~~ photoresist mask will be masked to etched for window for n-well



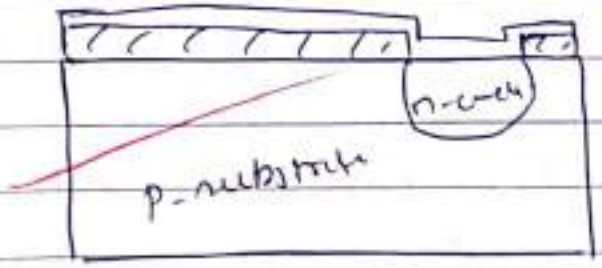
- The part or window required for formation of n-well will be etched and photoresist layer will be removed



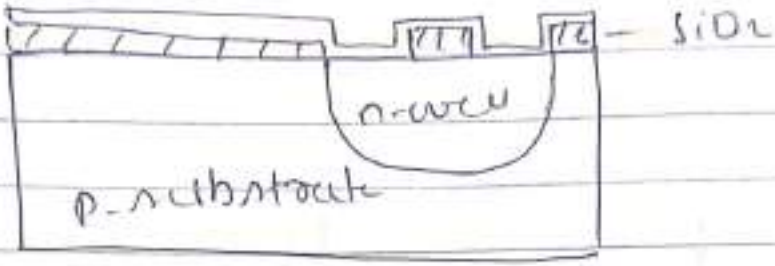
- Using ion-implantation and diffusion the n-impurities will be added which forms n-well



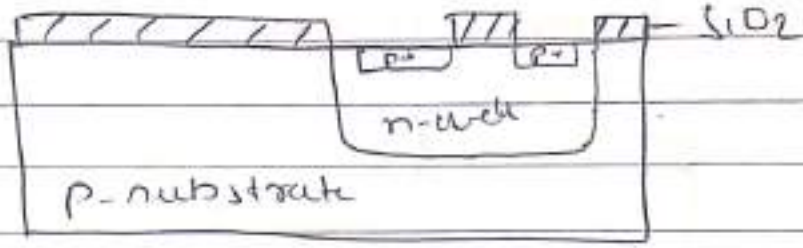
- Again the polysilicon layer will be formed above so that above further process should not damage the oxide other places



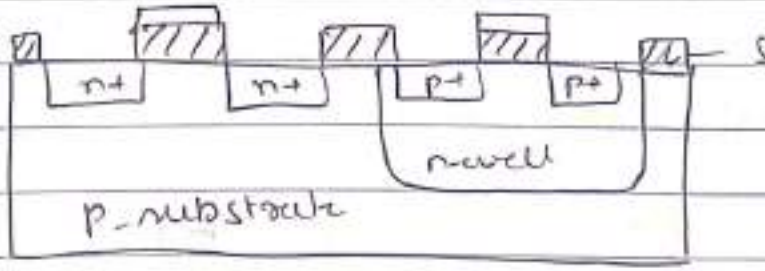
- Marking will be done using photoresist for the gate will be formed.



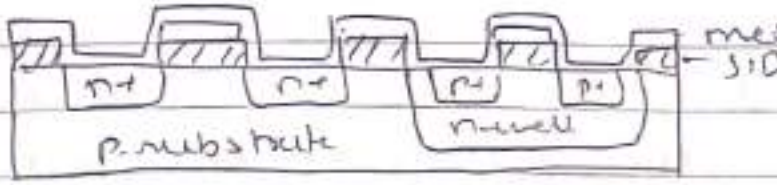
- Next we will be adding source and drain i.e. p+ with ion implantation and diffusion



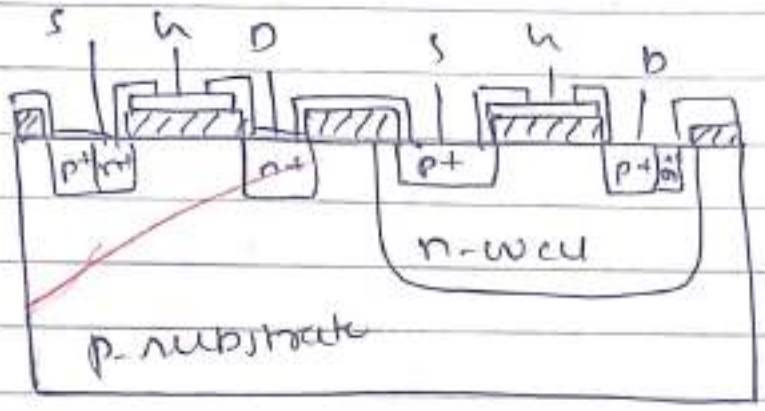
- similarly gate etching will be done for gate formation and source and drain for n-MOS



- finally after metalization will be performed over the wafer for metal contact



• etching will be done for removing the unwanted contact

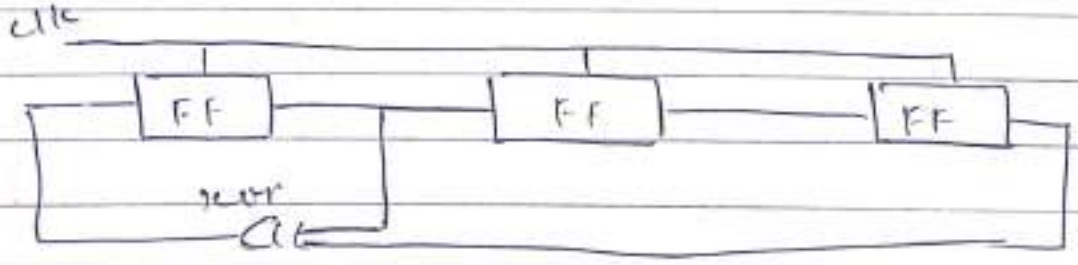


10

• Hence the formation of CMOS using n-well process is done

3.b BIST - Built in self test

• It is the test performed within in order to check the by generating random codes and thus this method is used



8 $fig = 1 + x + x^3$

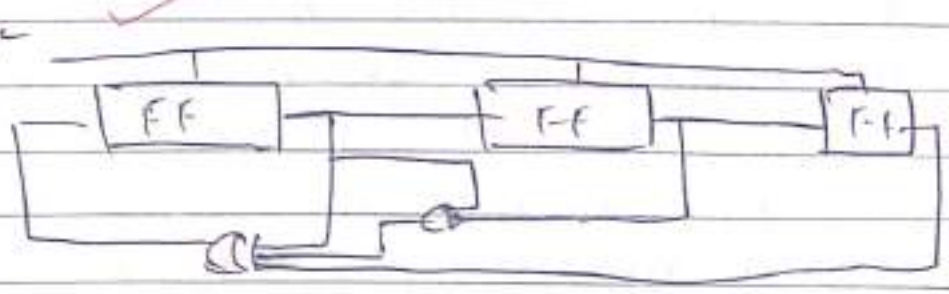


fig: PRSG

- The PRSG used is Read. Pseudo Random Sequence Generator
- where it generates the random sequence that is given to an i/p and O/p is observed and tested

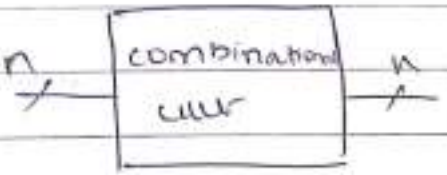
present state { 0 . . . 0 0
next state { 0 . . . 0 0 1

further after the procedure

present state { 1 0 0 . . . 0
next state { 0 0 . . . 0

3a. Manufacturing test principle:

- It is one of the main test principle performed prior to manufacturing of any IC's
- Let us consider a combination ckt which has n inputs and n outputs



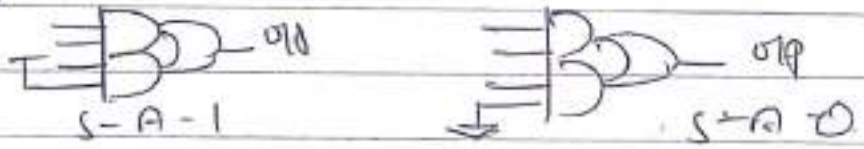
- The combination ckt will be converted to sequential ckt by adding registers in n hence it becomes $2^{(n+m)}$ I/p

- The principles are

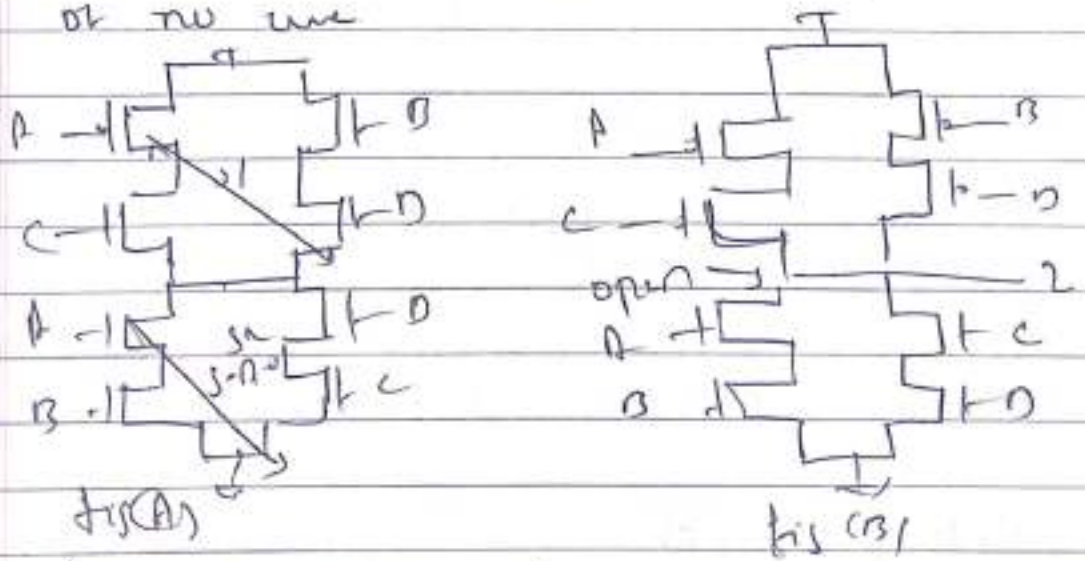
1. Fault model: It identifies where the fault is and its impact for a circuit

• The most commonly used are
(i) stuck at and (ii) short ckt / open ckt
(i) Stuck at can be of two types
stuck-at-2 (stuck-at-0 or s-a-0)
or stuck at one (stuck-at-1 or s-a-1)
It happens when nmos is connected to vdd and nmos is connected to gnd or any metal to metal contact happens

(ex)



(ii) short ckt / open ckt.
where there is short ie example s-a-0 in the fig circuit the o/p will be of no use



• fig (B) shows the open ckt when ~~then~~ is true. Here it converts combinational to sequential ckt and do more forth.

2 Observability

↳ It is observability where there is change in degree of node at o/p or and I/C and it is used to test large number of test pattern circuit o/p

3. controability:

It is the measure of ease of node changing the 1 to 0 state and it depends on the how the state can be changed

4. Fault coverage: It detects the fault occurance at the ckt or at the ckt and in its I/O or internal node which is controlled or controlled

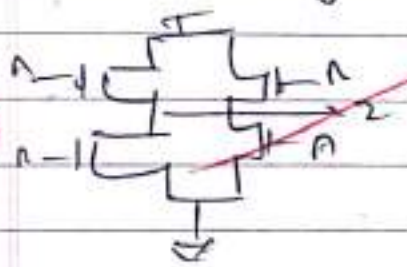
5. ATPh

↳ It is automatic test pattern generation where it automatic generates the test sequence for large or complex ckt that has to be tested

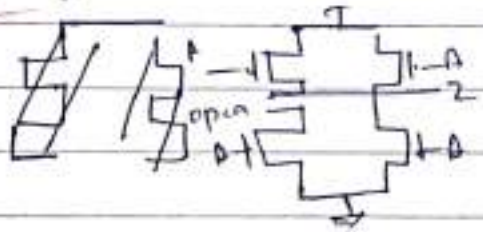
6. Delay fault:

↳ It is the one that occurs at ckt where when there is open ckt or anything like that it will just cause the delay but not alter the function of that circuit

for example consider a CMOS inverter when we open the det at one nmos then will be not much change or there will be no change in functionality expect there will only time change i.e delay is caused



CMOS inverter

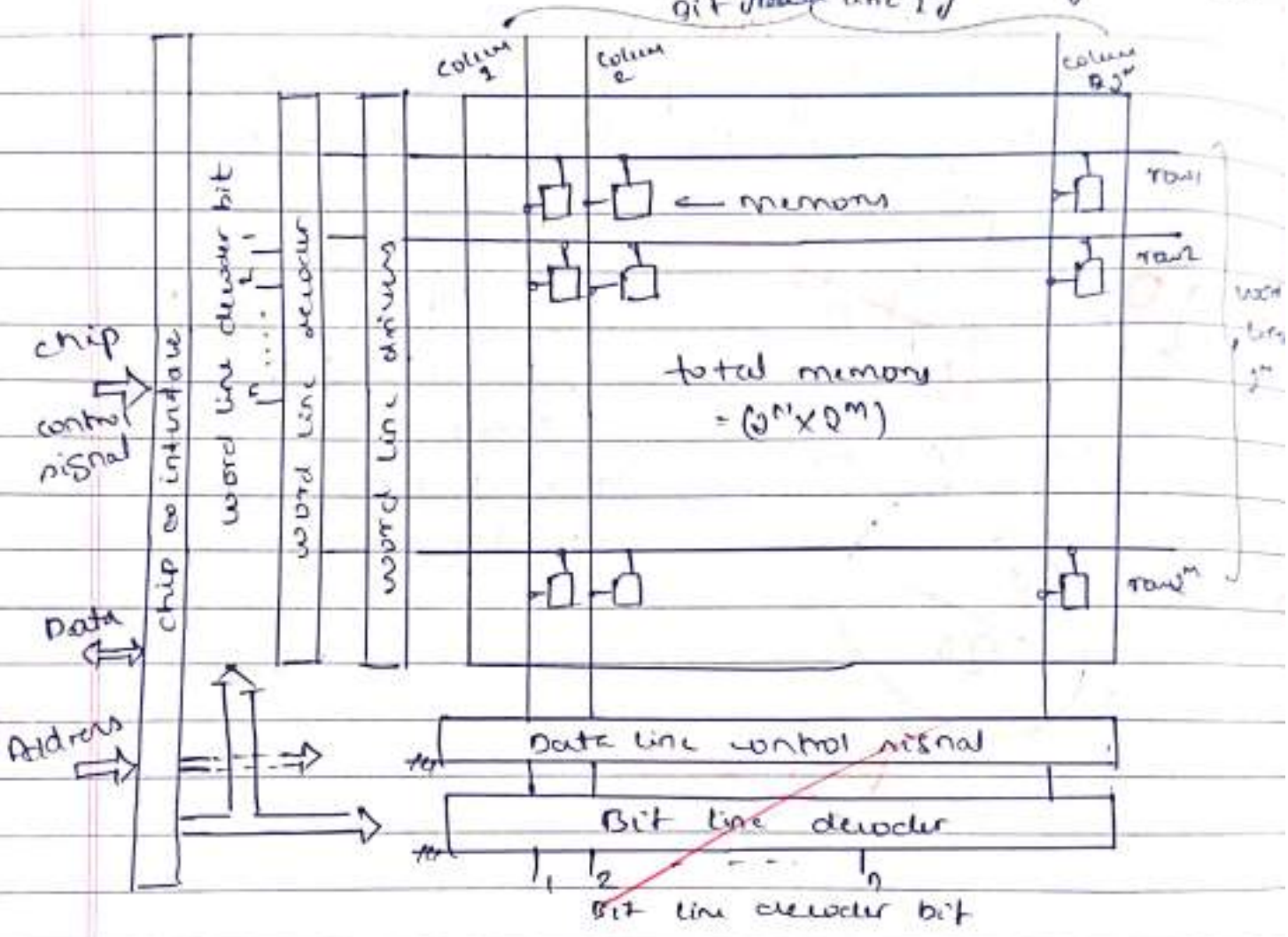


CMOS inverter with open at nmos which cause only time delay

27/01/2022

I.A - 03

1a. Random Access Memory Array Organization



- This is the arrray organization of Random Access Memory organization.
- It has total of $2^n \times 2^m$ memory cells in vertically as well as horizontally mannerly arranged order.
- There 2^m columns of bit lines and

2^N rows of word lines

- The memory cells row is connected to many other cells of same row and one column similary cells are connected in row to other rows cells in the same row and one in column.

- The memory cells in the block, each cell is connected to bit line and word line.

- Hence any cells can be accessed irrespective of the memory cell location.

- The word lines in row core connected to word line drivers that are connected to word line decoder where the input will be from external through word line decoder.

- Similarly bit lines in coloumn are connected to Data line control signal inturn connected to bit line decoder where input from external will will be through bit line decoder bit.

- And then whole thing is connected to chip interface where it will be controlled by chip control signal and the data in and the address bit from external should pass through this chip interface.

- Once the input is given from external i.e if the external has sent some address location.

- The row address is sent to bit line and word line decoder and through bit line and word line decoder bits.

- Decoder will decode and sends the location details to word line driver and data line control signal.

- They directly take that memory cells into consideration and perform necessary task i.e read and write operation.

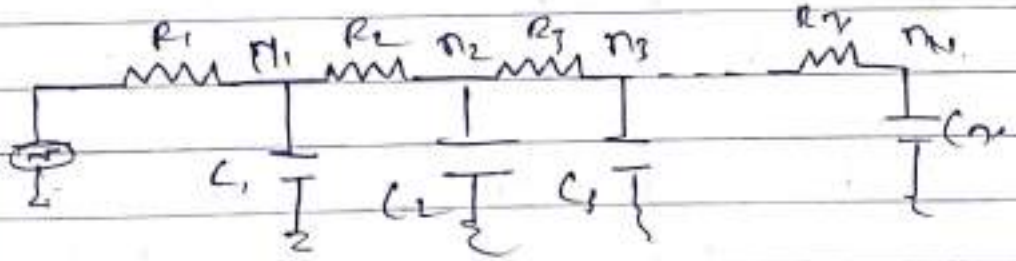
- Here, it is in the array form hence it is called as Random Access memory Array organisation.

4a.

Elmore Delay Model:

- Let us consider all the 'ON' transistor as resistor, and hence all the chain of transistor can be considered as RC ladder.

- Elmore delay model. estimates the delay of RC ladder as sum of the nodes at the ladder of resistance R_{n-1} present b/w node and source multiplied by the capacitance in RC ladder



$$t_{dp} = \sum_{i=1}^{n} R_i C_i$$

$$t_{dp} = \sum_{i=1}^{n} R_i \sum_{j=i}^{n} C_j$$

Linear Delay Model:

- The propapagation delay of the gate can be written as

$$d = f + p$$

p where, p → parasitic delay inherent gate when there is no load attached.

f → delay effort delay or state effort which is dependend on complexity and famiour

$$fd = gh$$

Where,

h → electrical effort or famour (for when h identical all of sates) when h is not identical to gate then

$$h = \frac{C_{out}}{C_{in}}$$ → capacitance at external load being driven

→ input capacitance of gate

let us good consider drive, i.e drive is reciprocal of resistance

drive : $1/f$

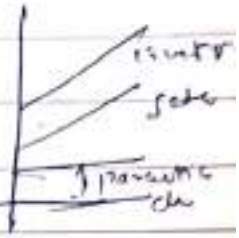
representing drive in terms of drive

$$d = \frac{C_{out}}{C_{in}} + d.$$

Logical effort : It is defined as ratio of i/p capacitance of gate to the ratio of i/p capacitance of inverter

denoted by g. where

$g = \frac{\text{slope of delay of gate}}{\text{slope of delay of inverter}}$



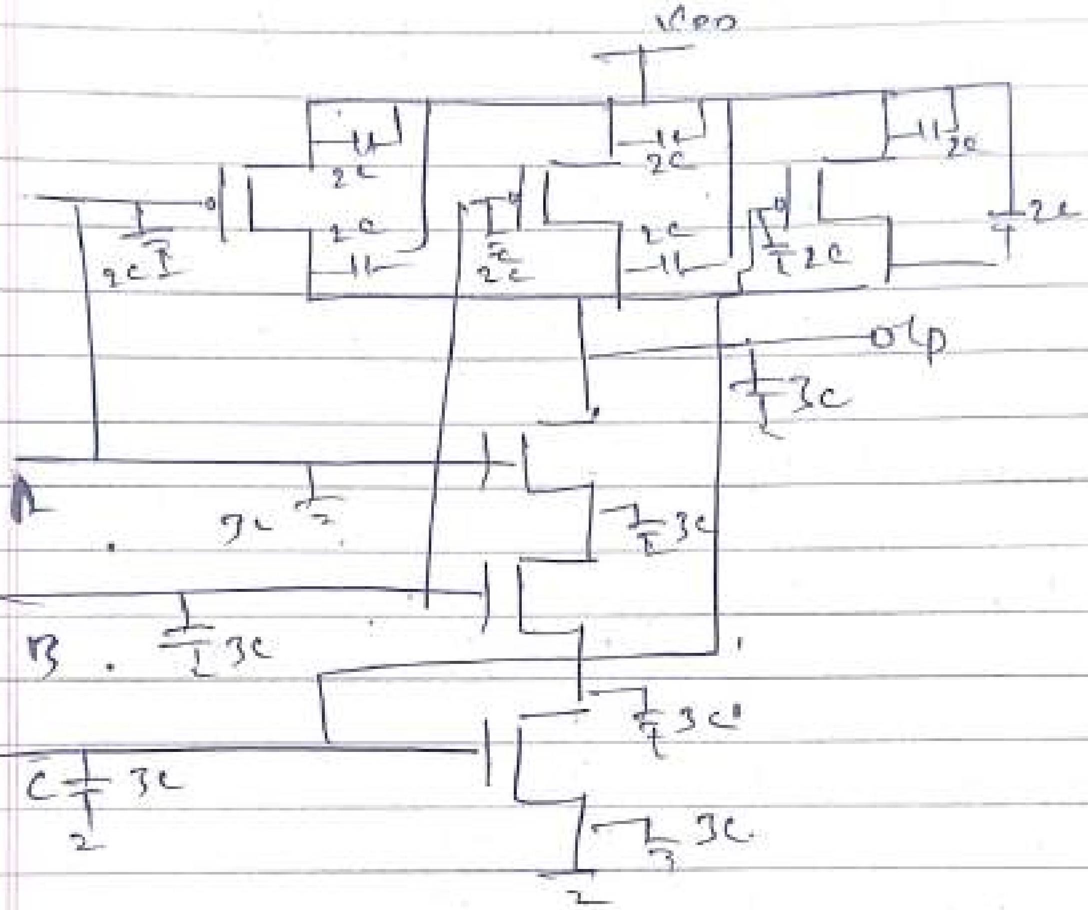
Logical effort for common gates,

type	i/p				
	1	2	3	4	n
inverter	1	-	-	-	
NAND	-	4/3	5/3	6/3	2n/3
NOR	-	5/3	7/3	9/3	(n+1)/3
tristate/mux	2	2	2	2	2
XOR / XNOR	4	4,4	6,6,6		

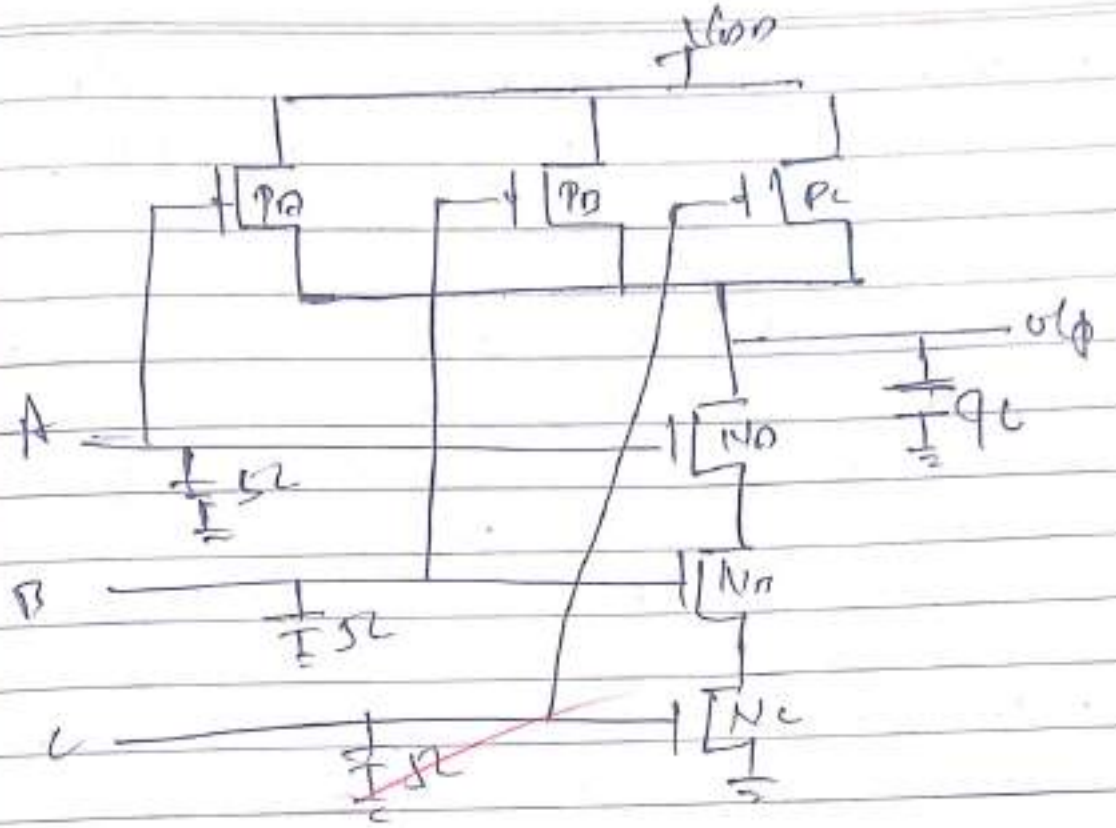
Parasitic delay :- It is define as delay of gate when drives a zero load and can calculated by rc delay model

	no of i/p				
	1	2	3	4	n
inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n
tristate	2	4	6	8	2n

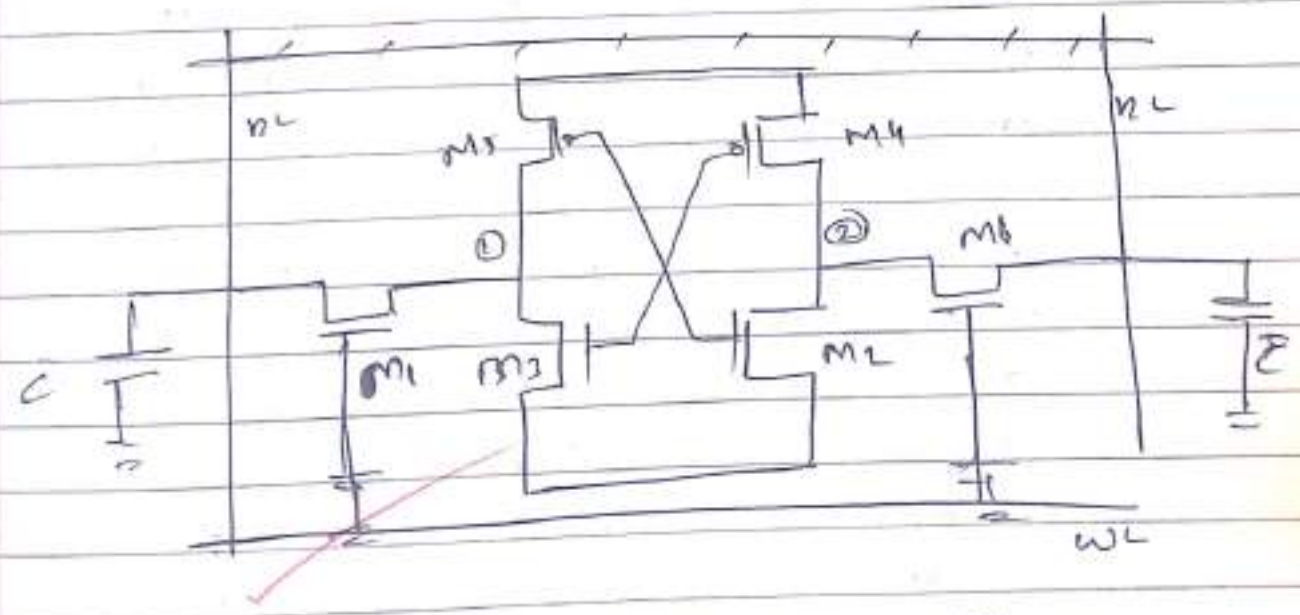
4b 3 input NAND gate w/L →
pmos → 2:1 , nmos - 3:1



i/p ~~sour~~/gate source is short here
at A, B, C → 2+3 = 5 and
output 2+2+2+3 = 9C
and the capacitance connected
to rail can be neglected.
Hence, the reduced circuit
will be



1.b. write operation of SRAM



- During write operation, there should be changes made in the SRAM compared to previous value

- When the input is 0 the voltage ① is Vdd and voltage ② is 0.
- When M1 and M6 are in active state. due to charge difference in capacitance C and voltage ② is different and capacitance C and voltage ① does not make any change
- The transistor M3 and M4 should be active, and voltage should be near or more than threshold value
- When voltage is more than threshold value the transistor M2 data i.e present in it will get corrupted and new data can be inserted
- The WL send the value to be high or low that has to be written and after the completion of that the input i.e the capacitance got discharged due to voltage ① and here the data is to be written to SRAM
- Hence the write operation takes place as mentioned in above process.